Asian Journal of Information Technology 5 (10): 1113-1116, 2006

Design of Low Power Double Edge Triggered D Flip Flop

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Abstract: A double edge triggered flip flop latches data at both edges of clock and hence it is advantageous over single edge-triggered flip flop in terms of power consumption and operating speed. Design of a low power Double Edge Triggered D Flip Flop (DETDFF) has been presented in this study and it is compared with two previously published DETDFFs for their performance and power consumption. The DETDFF circuits were simulated using TSPICE for 0.13 and 0.18µ technology CMOS process for different supply voltages. The proposed design is shown to have the lowest power consumption with respect to other double edge triggered flip-flops in all the above conditions.

Key words: Digital CMOS, double edge triggered flip flop, low power, low delay, VLSI

INTRODUCTION

A Single Edge-Triggered (SET) flip- flop, transfers data from input to output at one edge of the clock, either at positive edge or negative edge, whereas the Double Edge-Triggered (DET) flip-flops transfers data at both the edges of the clock. Even though DET flip-flops have more complex structures, occupying larger silicon area compared with its SET counterpart, the clock frequency can be made one half for a given throughput, in comparison with a system using SET flip-flops. This leads to a reduction in power consumption and hence can be very well used for low power applications[1-4].

Design of low power circuits has become an important criteria in the modern VLSI CMOS technology, due to the massive usage of portable battery operated, computing and communication systems. Apart from low power consumption, another important factor to be considered is the speed. To have high performance ICs, the delay involved in the circuit should be as low as possible. However, both these factors tends to diverge in deep sub micron technology designs[5].

In this study a simple, less complex Double Edge-Triggered D Flip-Flop (DETDFF) has been presented to satisfy both the criteria, the low power consumption and lower delay. The proposed DETDFF has been compared with DETDFFs designed by Gago and Wai chan[2,3] in terms of power consumption and delay. In his work[3], had compared 4 circuits and concluded that his circuit has least delay in low voltage applications whereas Gago circuit excels in both low power consumption and lower delay in nominal conditions. Hence both these circuits have been selected for comparing with the proposed DETDFF. The proposed circuit has been simulated for different supply voltages for 0.13 and 0.18µ technologies and compared for its performance with Gago and Wai Chung circuits.

EARLIER DETDFFS

Gago DETDFF: DETDFF designed by[2] is shown in Fig. 1.

In this circuit, the upper stage issues output at negative edge of clock and lower stage issues output at positive edge of the clock. The nodes N2, N3, N4 and N5 activates and deactivates the upper and lower stages according to the phase of the clock. The perfect isolation of active and inactive parts provides low power consumption but it leads to higher delay. The circuit requires 22 transistors.

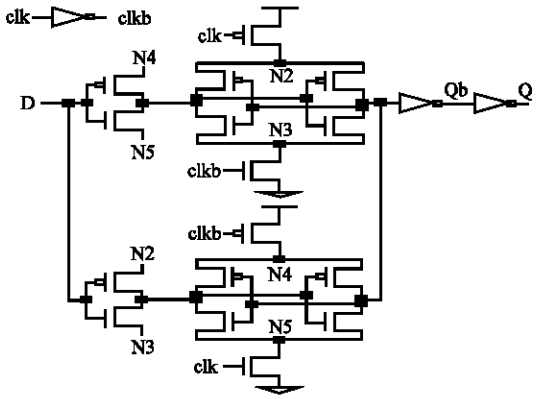

Fig. 1: DETDFF-Gago

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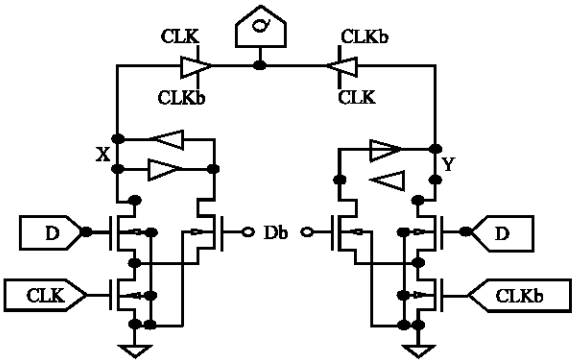

Fig. 2: DETDFF-Wai Chung

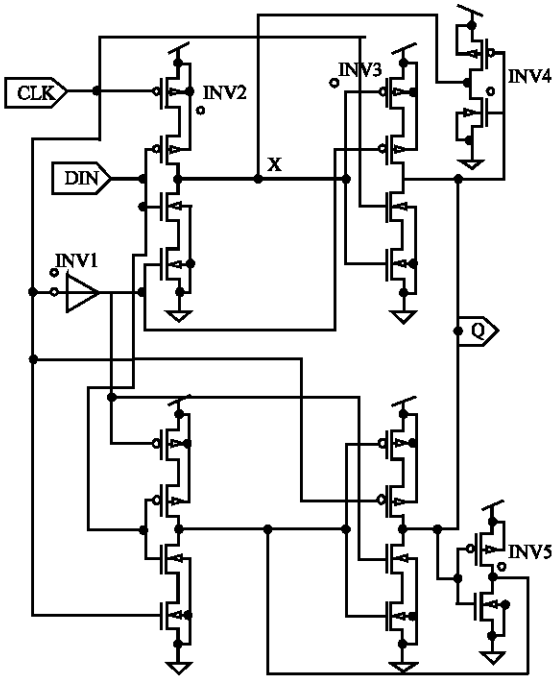

Fig.3 : Proposed DETDFF

Wai chung- DETDFF: DETDFF designed by[3] is shown in Fig. 2. According to the actual and complement values of clock, the two stages of the circuit latches data at the edges of the clock. As this circuit avoids the stacking of PMOS transistors, it is suitable for low voltage applications. But since the circuit has 26 transistors, the power consumption is slightly higher. Due to the usage of Pass transistor logic, the delay is also higher.

PROPOSED DETDFF

Figure 3 shows the proposed DETDFF. Similar to the above circuits, the proposed DETDFF has also two stages: The upper stage, issuing output at positive edge and lower stage at negative edge. The upper stage operates as follows : If CLK = 0 and data input DIN = 1, then both the NMOS in the INV2 inverter circuit are ON, and hence the node X is pulled down to 0. However the inverter INV3 will not respond until CLK remains 0. At the positive edge of the clock, the INV3 responds and since X = 0 the output Q will rise to 1.

For DIN=0 and CLK=0, both the PMOS in the INV2 inverter circuit are ON, and hence X rises to 1. At the positive edge of the clock, INV3 responds and since X = 1, the output Q falls to 0. Until CLK remains in 1, the change in DIN will not have any effect over the output as INV2 will be inactive.

Similarly the lower stage issues output at negative edge of the clock. The inverters in the feedback path of each stage act as staticizers. The proposed circuit requires 22 transistors.

SIMULATION RESULTS

For low power applications, the power consumption should be minimum, whereas for high performance circuits, the delay should be as low as possible. Since the objective is to construct a DETDFF to have low power consumption and lower delay, we have considered the parameters, power consumption, delay and power delay product for comparing the proposed circuit with other DETDFFs. All the DETDFFs have been simulated using TSPICE for 0.13 and 0.18 μ CMOS technology. The clock frequency is set at 1 GHz and 10 data bits sequence is applied. The rise and fall times of both data and clock signals are set as 0.1ns. The 0.13 μ circuits were simulated with Vdd at 1.3, 1.0 and 0.8v, whereas the 0.18 μ circuits for Vdd at 1.8 and 1.5v.

In order to verify the performance of the proposed DETDFF for a wide range of data activities, the simulation is carried out at different data activity rates $\alpha = 0$ (all zero's and all one's), 0.5(alternate 1's and 0's) and 1(successive 1's and 0's- 110011…). The data change is done 0.2 ns before the edges of the clock thus satisfying the setup time requirement.

Following[3,6,7], to verify the performance under different load conditions, we have simulated 0.13 μ DETDFF circuits with a fan out of 4 inverters each driving a capacitive load C_L of 5fF. The 0.18 μ circuits were simulated with fan out of 3 inverters each driving C_L of 1.5fF. In both the above conditions, we have loaded input DIN with two buffers followed by capacitive load C_L. Table 1-3 give the simulation results for the DETDFFs for different data activity rates in 0.13 μ technology with supply voltages 1.3, 1 and 0.8v, respectively. Table 4 and 5 show the simulation results for 0.18μ DETDFF

Table 1 : 0.13 μ - Vdd = 1. 3v

DETDFF Circuit	Power consumption (μ w) α = 0 (all 0)	α = 0 (all 1)	α = 0.5	α = 1	Delay (ps)	Power delay product (fJ)
Gago	4.564	8.503	61.27	32.90	184	11.273
Wai Chung	9.132	12.350	52.08	36.09	165	8.593
Proposed	10.140	2.974	41.59	22.55	158	6.571

Table2 : 0.13 μ - Vdd = 1. 0 v

DETDFF Circuit	Power consumption (μ w) α = 0 (all 0)	α = 0 (all 1)	α = 0.5	α = 1	Delay (ps)	Power delay product (fJ)
Gago	1.989	3.379	29.20	15.26	221	6.453
WaiChung	4.840	1.770	33.86	15.02	196	6.636
Proposed	5.360	1.637	21.68	12.60	189	4.097

Table 3 : 0.13μ - Vdd = 0. 8v

DETDFF Circuit	Power consumption (μ w) α = 0 (all 0)	α = 0 (all 1)	α = 0.5	α = 1	Delay (ps)	Power delay product(fJ)
Gago	0.834	1.510	15.59	8.211	226	3.523
WaiChung			Failed			
Proposed	3.040	0.509	12.12	6.728	216	2.617

Table 4 : 0.18μ - Vdd=1.8v

DETDFF Circuit	Data rate α = 0.5 Power consumption (μ w)	Delay (ps)	Power delay product (fJ)
Gago	124.50	182	22.660
WaiChung	111.70	193	21.558
Proposed	89.58	35.5	21.096

Table 5 : 0.18μ - Vdd=1.5v

DETDFF Circuit	Data rate α = 0.5 Power consumption (μ w)	Delay (ps)	Power delay product (fJ)
Gago	68.27	198	13.517
WaiChung	74.05	226	16.735
Proposed	55.70	269	14.983

Table 6: Comparison with Yu-Yin Sung circuit

DETDFF	Power consumption (μ Watts)
Yu-Yin Sung	47.80
Proposed	8.290

circuits for α = 0.5 with Vdd = 1.8v and 1.5v, respectively. Here, the power consumption refers to the average power consumption by the DETDFF circuit and the delay to the time measured between the clock edge and output edge. The power delay product is obtained as the product of power consumption for α = 0.5 and delay.

From Table 1-3 (0.13 μ technology), for all 0 input condition, the Gago circuit has least power consumption where as the proposed circuit has higher power consumption. But the occurrence of this data sequence with continuous 0's is less and hence it may not be a significant drawback for the proposed DETDFF. But for all the other data activity conditions with Vdd = 1.3, 1 and 0.8v, the proposed circuit dominates both Gago and Waichung circuits in terms of power consumption and delay. With Vdd = 0.8v, the Waichung circuit failed. The Fig. 4 gives the output waveform for the proposed DETDFF in 0.13 μ technology, for α = 0.5 with Vdd = 1.3v. In the figure, the first marker is at 2.705ns indicating the negative edge of the clock (DIN is at 1 at that instant) and the second marker is at 2.863ns, where output Q reaches logic 1. Having a close look, we can observe the value of dx = 157.75ps which is taken as the delay time between CLK edge and output Q. In Table 1, this value is approximated and shown as 158ps. From Table 4 and 5, we can infer that, in 0.18 μ technology, the proposed circuit dominates other circuits in having lower power consumption but has higher delay for both the supply voltages 1.8 and 1.5v.

The results indicates that, even though the proposed circuit has same number of transistors as in Gago and slightly less number of transistors as in Wai Chung, it consumes low power and has lower delay in 0.13 μ technology whereas low power consumption and higher delay in 0.18 μ technology, compared with them.

Further comparing the proposed circuit, with the DETDFF designed by Yu Yin[7], the result confirms that the proposed design stands ahead in low power consumption. Yu-Yin Sung had simulated the circuit in 0.18 μ technology with Vdd = 1.5v for 125Mhz clock frequency with α = 0.5. For the above simulation condition, the power consumption of his circuit, according to him is 47.8 μ Watts, where as the proposed design has a power consumption of 8.29 μ Watts Table 6.

CONCLUSION

In this study, the design of a simple Double edge Triggered Flip Flop is presented. The proposed design has been compared with the two previously published Double Edge Triggered Flip Flops for their performance and power consumption. For each DETDFF the optimal delay and power consumption are determined as the primary figure of merit. The DETDFF circuits designed by Gago and Wai Chung along with the proposed circuit were simulated using TSPICE for 0.13 and 0.18 μ technology CMOS process under different supply voltage conditions and load conditions. The simulation results show that the proposed design in 0.13 μ technology has least delay and lowest power consumption and hence lower power delay product with respect to other double edge triggered flip-flops. The power consumption has

been reduced by at least 21% and the power delay product is reduced by 24%. Thus the goal of designing a DETDFF satisfying both the criteria of lower power and lower delay has been attained. Whereas in 0.18 μ technology, the proposed circuit has least power consumption (reduced by 20%), but has more delay. But the power delay product is on par with the other two designs. Hence the proposed circuit operates more efficiently in 0.13 μ technology and suits well for applications where power consumption is critical.

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