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Design and Implementation on DSP of a Frequency Synthesizer

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Abstract: Digital synthesizers of frequency are used extensively in most technological domains as the instrumentation, the communication and the modern telecommunications systems. In this study, one proposes to present some techniques of frequency synthesis in these two analog and digital forms. The three basic synthesis techniques are namely direct analog synthesis, direct digital synthesis and indirect analog synthesis. For the case of frequency indirect synthesis, we have used the technique of Phase Locked Loop PLL in frequency synthesizers design such as, for example, fractional-N PLL synthesizers and sigma-delta fractional-N PLL's synthesizers. We have also proposed and studied a digital frequency synthesizer functioning as a digital oscillator to controlled amplitude and frequency. The conceived synthesizer was built from the discretization of sine function. The gotten algorithm has been implemented on the SHARC EZ-KIT Lite, based around the ADSP-21065L Digital Signal Processor DSP. The algorithm has been applied to the amplitude modulation and the frequency. The satisfactory results of implementation have been presented and discussed in various cases in the goal to validate the analytic study features.

Key words: PLL systems, frequency synthesis systems, analog and digital synthesis, hybrid synthesizers, controlled digital oscillator, digital signal processor DSP

INTRODUCTION

During these last years and with the technological development increased in the signal numerical treatment domain, different techniques of frequency synthesis saw the day. To the departure, the principle was based on analogical techniques. However, thanks to the profit that one can have in the use of the numeric, the schemes of synthesis have been built in digital form as implemented algorithms on dedicate processor.

Many techniques are used in frequency synthesizers design. The technique of Phase Locked Loop PLL has been the more well known especially in telecommunications domain (Abramovitch, 2002; Gardner, 1979; Hseih and Hung, 1996). In fact, the use of wireless products has been rapidly increasing in the last years thanks to the advanced technology in the fabrication of Digital Signal Processors DSP (Ahola, 205; Kim *et al*., 2003).

In this study, we first present some techniques of frequency synthesis in analog and digital forms: Direct analog synthesis, direct digital synthesis and indirect analog synthesis. In this context, " indirect" refers to a system based on some kind of a feedback action, whereas "direct" refers to a system having no feedback.

Examples of hybrid synthesizers are also presented: N PLL synthesizers and sigma-delta fractional-N Phase Lock Loops PLLs synthesizers (Perrott, 2002; Perrott *et al*., 2002). We propose, in this study, an architecture of a frequency digital synthesizer of the direct type whose constituent elements are then:

- The controlled digital oscillator in amplitude and in frequency.
- The Digital Signal Processor DSP.
- The Analog Digital Converter ADC.

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FREQUENCY SYNTHESIS TECHNIQUES

The basis function of a frequency synthesizer is the fact to have need no of an unique frequency but of various different frequencies, spaced regularly (sampling step of the synthesizer) and having a good accuracy and stability. As mentioned, one distinguishes mainly two synthesizers types:

- The synthesizers to analogical character.
- The synthesizers to numeric character.

Analog synthesis: The basis principle of an analogical frequency synthesizer uses the synthesis of frequency according to two processes direct and indirect.

Direct analog synthesis: The direct synthesis technique is based on the division and on the multiplication of the frequency via two independent circuits dedicated to these two functions, these two frequencies are mixed then and filtered by a high pass filter. We use a crystal reference of high stability for giving the reference frequency which assures the principle of the desired function. The scheme of Fig. 1 illustrates the principle of this direct synthesis method.

The direct synthesis is efficient enough but implies many circuits what makes it expensive. It gives a synthesized frequency lower than the higher input frequency. Therefore, its use in high frequency applications is quite limited. Also noise is an important problem (noise of the mixers, filters and dividers). So, the use of direct analog synthesis is limited to low frequencies and to applications which are not too sensitive to noise (Ahola, 2005; Grawford, 1994).

Indirect synthesis: use of a PLL: One exploits again here a crystal oscillator for a reference of stability and one associates it to a Voltage Controlled Oscillator VCO. The VCO delivers a frequency whose value is proportional to the command voltage. The idea is to enslave artfully the frequency of the oscillator to the one of crystal with a near multiplier coefficient, which can be modified comfortably.

PLL based frequency synthesizer: The block diagram of a Phase Locked Loop PLL operating as a frequency synthesizer is shown in Fig. 2. It consists of these following components:

- A reference OSCillator OSC
- A Phase/Frequency Detector PFD
- A Charge Pump CP

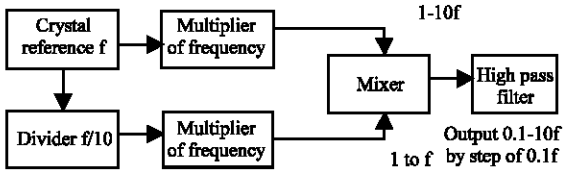

Fig. 1: Principle of direct synthesis method

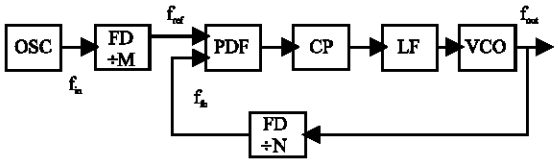

Fig. 2: The block diagram of a PLL operating as a frequency synthesizer

- A Loop Filter LF
- A Voltage Controlled Oscillator VCO
- Two Frequency Dividers FDs

The PLL is a feedback loop that, when in lock, forces f_{fb} to be equal f_{ref}. Given a reference frequency f_{in}, the frequency at the output of the PLL which is equal to N/M* f_{in}.

The choice of frequency divide ratios and input frequency permits to the synthesizer to generate an output signal at the desired frequency that inherits much of the stability of the reference oscillator. In Radio Frequency RF transceivers, the synthesizer is used to generate the Local Oscillator LO at programmable frequency, which is made by the adjustment of the value of N (Gardner, 1979; Girard, 1988; Heish and Hung, 1996).

Fractional-N PLL synthesizer: The basic operation of N PLL synthesizer consists on an integer N PLL. The block diagram of this shape of synthesizers is shown in Fig. 3 where N is an integer (N = 4501). When N is chosen as a fractional counter(N = 900 1/5 for example), then we have a fractional-N PLL synthesizer (Fig. 4).

Fractional-N synthesizers offer technical advantages required for next generation telecommunication hardware. Kim *et al.* (2003) gives a study in simulation using behavioral blocks which offer key architectural design capabilities.

Sigma delta fractional-N Phase Lock Loops PLLs synthesizer: In the last decade, the use of wireless products has been rapidly increasing and there has been world wide development of new systems to meet the needs of this growing market (Ahola and Crawford, 1994). As a result, new radio architectures and circuit techniques are being actively sought that achieve high levels of

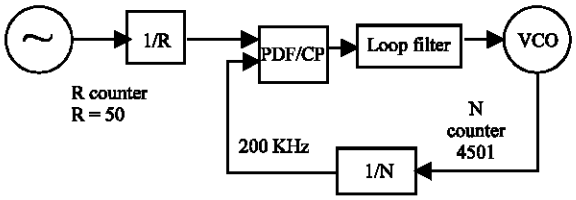

Fig. 3: Basic operation of integer N PLL Synthesizer

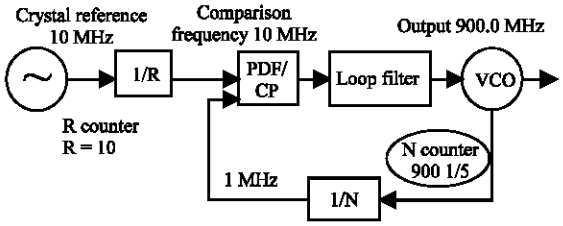

Fig. 4: Basic operation of a Fractional N PLL Synthesizer

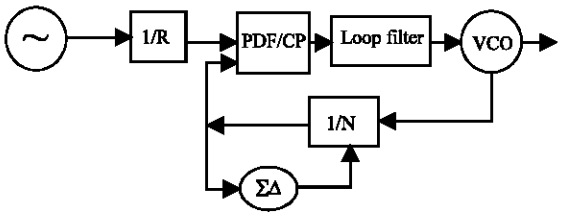

Fig. 5: Sigma delta fractional-N PLLs synthesizer

integration and low power operation. They response well to the straight performance requirements of radio systems today. The use of Sigma-delta modulation achieve high-resolution frequency synthesizers (Parrott *et al*., 2002). In contrast to classical Phase Locked Loop PLL systems, a Sigma-delta synthesizer dynamically varies the divide value in the PLL according to the output of a sigma-delta modulation as shown in Fig. 5. This shape of synthesizer is most beneficial for applications with narrow channel spacing (100 kHz):

- Tighter channel spacing than integer-N PLLs
- Improved (lower) spurious response
- Improved phase noise performance
- Allows wider loop bandwidths for faster lock times.

Digital synthesis: The digital synthesis can be landed according to two processes direct and indirect.

Direct digital synthesis

Direct synthesis by converter: The idea of basis consists in exploiting the principle of Analog Digital Converter ADC piloted by a micro-controller. Indeed if one sends to the ADC input a digital information following in the time a sine type evolution, the ADC output is going to provide a sine appreciably analogical signal that will be sufficient to make pass in transit by a relatively simple filter; then we obtain a perfect sine signal as shows the diagram of the Fig. 6.

Direct digital synthesis to basis of DRM: This method of synthesis is simple and calls on classic logical components. The Decimal Rhythms Multiplier DRM is a very particular frequency divider which possesses an input, two outputs and a command input K receiving a word of 4 bytes from 0000-1001. The Fig. 7 illustrates the operating of the DRM for K = 5.

To achieve a frequency synthesizer based DRM as shows the Fig. 8, it is sufficient to place several DRM in series, the P signal of each of them constitutes the clock signal E for the next one: While inserting a divider by 100, the middle frequency is divided by this same rate. The jitter of the transitions to the counter output remained the same, however it represents the 1/100 of the period.

Indirect digital synthesis: The indirect digital synthesis calls on the technique of a digital PLL system as shows the diagram of the Fig. 9. In this technique, it is about a phase detector to Digital Analogical Converter DAC, the Fig. 10 illustrates the use of the digital PLL in the digital synthesis of frequency. In this study, one has evoked some techniques of frequency synthesis so much in analogical that in numerical.

To conclude, one can affirm that there are a lot of other techniques of frequency synthesis applied to the sound synthesis: One can mention the synthesis to surface acoustic wave which is based on the use of the filters in comb selected by commutation and permitting to get harmonic components of the frequency of the broadcast. The advantage of this synthesis method is the speed of the commutation for merely some decades of available frequencies. There are also other types of synthesis, the subtractive and additive methods. These last are specially used in the resonant frequency synthesis (Organs to harmonic zippers).

We propose the design of a digital synthesizer based on the discretization of sine function. We have implemented on DSP the recursive algorithm permitting to generate a sine signal where the synthesized frequency and the amplitude are chosen by the action on two parameters and the initial conditions. Various curves illustrating the synthesizer function-nement will be presented and discussed.

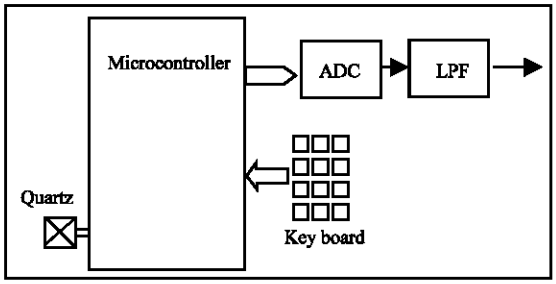

Fig. 6: Direct digital synthesis by ADC converter

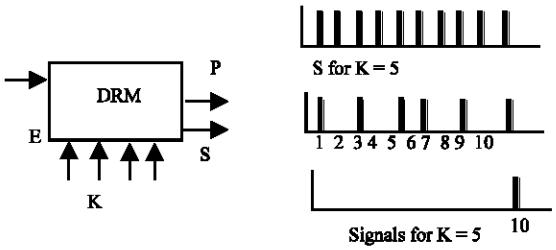

Fig. 7: Decimal Rhythms Multiplier DRM

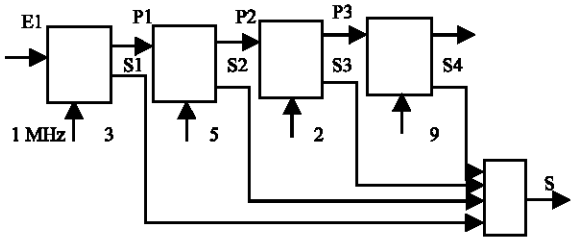

Fig. 8: DRM Synthesizer

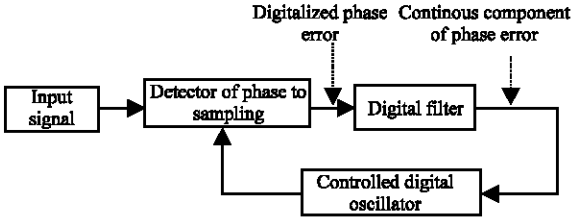

Fig. 9: Synoptic scheme of a PLL

DESIGN OF A DIGITAL OSCILLATOR FUNCTIONING AS A SYNTHESIZER

The idea of departure is to establish a recursive algorithm permitting to generate numerically the sine signal while controlling its amplitude and its frequency. It is the controlled digital oscillator.

Indeed, let's consider the sinusoidal signal x(t) with a pulsation $\omega_0=2\pi/T_0$.

Its discrete form:

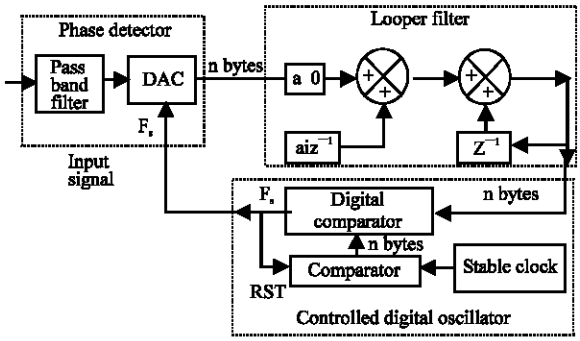

Fig. 10: The use of digital PLL in frequency synthesis

(x k = kα where) $\alpha = 2\pi T_e/T_0$, T_e: Period of sampling

$$\text{Then } x(k+1) = x(k)\cos(\alpha) + \cos(k\alpha)\sin(\alpha) \quad (1)$$

$$\cos((k+1)\alpha) = \cos(k\alpha)\cos(\alpha) - x(k)\sin(\alpha) \quad (2)$$

From a simple trigonometric computing, it is possible to formulate the numerical sinusoidal output under the shape of the following recurrent equation:

$$x_k = 2\cos(\alpha)\, x_{k-1} - x_{k-2} \quad (3)$$

With,

$$\alpha = 2\pi T_e/T_0 = 2\pi . f_0/f_e \; ; \; f_0/f_e = k/N$$

The features of the desired signal are fixed by the choice of the following parameters:

- The initial conditions x_0 and x_1.
- The coefficient a given by the formula $a = 2\pi.k/N$.

N is the number of treaties samples and k is the number of the computed periods of the signal in N samples.

The analysis of the digital frequency synthesizer with the recurrent equation permits to identify the signal in frequency and amplitude.

IMPLEMENTATION ON DSP OF THE DIGITAL FREQUENCY SYNTHESIZER

In the objective to validate our theoretical survey, we have implemented the recurrent algorithm of the synthesizer on the Super Harvard Architecture Computer "SHARC EZ-KIT Lite", based around the "ADSP-21065L" Digital Signal Processor of ANALOG-DEVICE to 32 bytes. Its architecture is composed of five blocks:

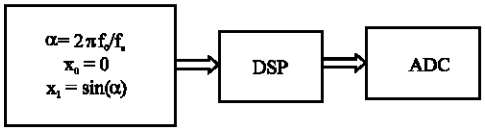

Fig. 11: The device adopted for the generation of a sinusoidal signal

- The heart of the processor (ALU, MBS, DAG1,DAG2)
- Two independent blocks Synchronous Read Access Memory SRAM
- A block of test and emulation JTAG.
- An external port (constituted of a master port and SDRAM interface).
- A block of inputs/outputs (composed of a DMA controller and registers).

The device adopted for the generation of a sinusoidal signal is illustrated by the following Fig. 11.

According to the features wanted of the sine signal, one fixes the initial conditions x_0, x_1 and the parameter a of the recursive Eq. 3.

RESULTS AND DISCUSSION

We recall that the recursive recurrent Eq. 3contains a coefficient of the shape cos(a) whose value is understood between-1 and 1.
First of all, we study the following particular cases:

First case: For $\cos(\alpha) = 0$ one has $x_0 = 0$, $x_1 = 1$. The recurrent Eq. 3 is written as $x_n = -x\, n_{n-2}$. The curve of the Fig. 12 shows the result of implementation.

Second case: For $\cos(\alpha) = \pm 1$ one has $x_0 = x_1$, the recurrent Eq. 3 becomes: $x_n = 0$. For all values of $\cos(\alpha)$ different from these treated cases; the recurrent Eq. 3 permits to generate a sinusoidal signal.

Third case: We fixed in this case k = 5 and N = 720, with $x_0 = 0$ and $x_1 = \sin(\alpha)$, where, $\alpha = 2\pi k/N$, the in Fig. 13 curve shows the signal gotten in the output of the oscillator.

One notices that the period of the signal is equal to N/k report (144 s).

Fourth case: For k = 8 and N = 720 with $x_0 = 0$ and $x_1 = \sin(\alpha)$, where, $\alpha = 2\pi k/N$, the following curve illustrates the signal gotten in the output of the oscillator (Fig. 14).

One notices here that the period of signal has changed to "720/8 s". For studying the influence of the

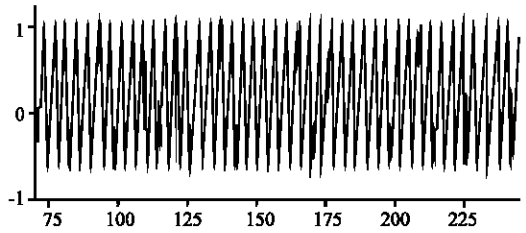

Fig. 12: The output signal for $\cos(\alpha) = 0$ ($x_0 = 0$ and $x_1 = 1$)

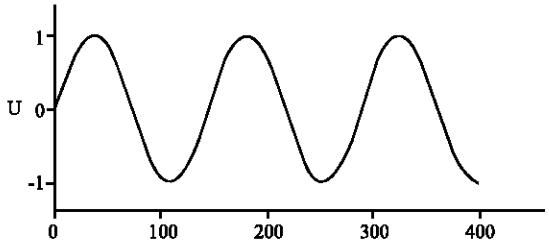

Fig. 13: The output signal for N = 720 and k = 5 ($x_0 = 0$ and $x_1 = \sin(\alpha)$)

initial conditions on the characteristic of the signal in the output of the digital oscillator (k = 5 and N = 720), two schemes are suggested. In two first cases, one modified the value of x_1 (x_0 being maintained constant) and in the two other cases, one changed the value of x_0 (x_1 = constant).

x_0 being maintained constant, x_1 variable: x = 0, k = 5 and N = 720 for x_1 = 0.1, 0.2 and 0.3, the following curves illustrate the found result (Fig. 15).

With $x_0 = 0$, k = 5 and N = 720 for x_1 = 0.2, 0.4 and 0.6, the gotten result is shown in the Fig. 16.

According to the result of the implementation, one notices that the magnitude variation of the signal output is linearly proportional to the variation of the initial conditions x_1 ($x_0 = 0$).

x_1 being maintained constant, x_0 variable: $x_1 = \sin(2\pi 5/720)$ for x_0 = 0.1, 0.2 and 0.3, the following curves illustrate the gotten result (Fig. 17).

With $x_1 = \sin(2\pi 5/720)$, for x_0 = 0.2, 0.4 and 0.6, the curves are represented in the Fig. 18.

According to the result of the implementation, one also sees that the amplitude of the signal output is linearly proportional to the variation of the initial condition $x_0(x_1=\sin(a))$. One can conclude from these results t hat the controlled digital oscillator as designed is a digital synthesizer of frequency permitting to generate any frequency while simply introducing of k and N. It is to note that the N parameter fixes the range of frequency of the synthesizer whereas k fixes the step.

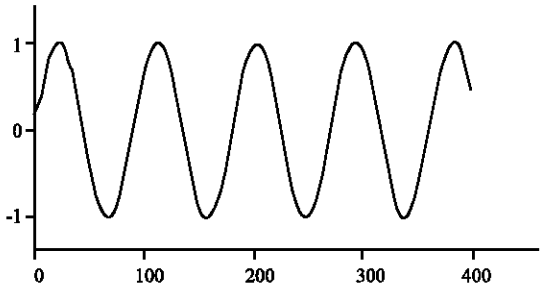

Fig. 14: The output signal for N = 720 and k = 8 (x_0 = 0 and x_1 = sin (α))

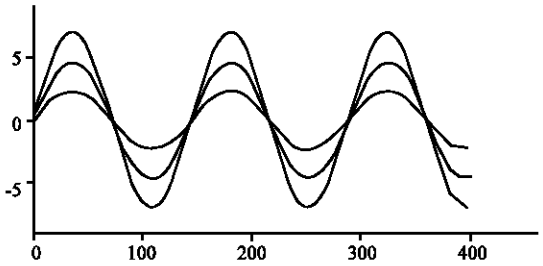

Fig. 15: Influence of x_1 on the signal level for k = 5 and N = 720 (x_0 = 0 and x_1 = 0.1, 0.2, 0.3)

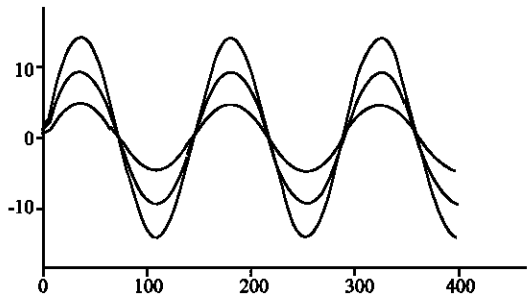

Fig. 16: Influence of x_1 on the signal level for k = 5 and N = 720 (x_0 = 0 and x_1 = 0.2, 0.4, 0.6)

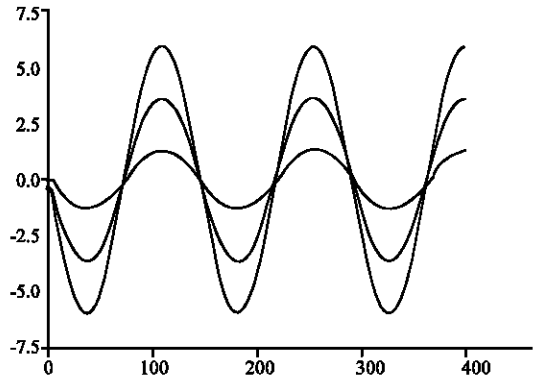

Fig. 17: Influence of x_0 on the signal level for k = 5 and N = 720 $(x_1 = \sin(\frac{2\pi.5}{720}); x_0 = 0.1, 0.2, 0.3)$

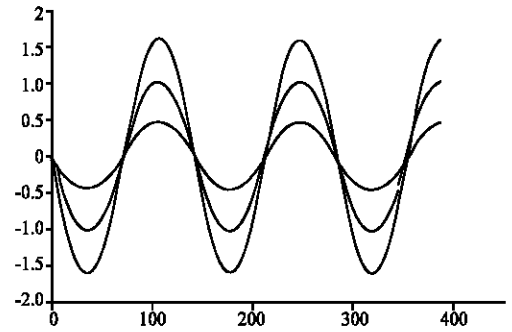

Fig. 18: Influence of x_0 on the signal level for k = 5 and N = 720 $(x_1 = \sin(\frac{2\pi.5}{720}); x_0 = 0.2, 0.4, 0.6)$

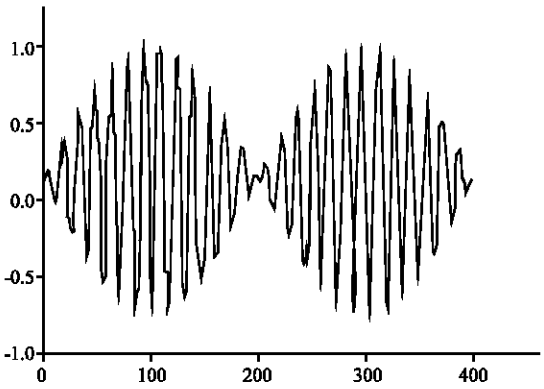

Fig. 19: Application to the amplitude modulation Concerning the following figure in the manuscript, the title is: Application to the frequency modulation

APPLICATION OF THE SYNTHESIZER TO THE AMPLITUDE MODULATION AND THE FREQUENCY

One applied the algorithm (E) to the digital transmission domain. In fact for modulation of amplitude, the bearer's frequency is chosen according to the nature of the considered application and according to the distance of the receiver. The principle of the modulation of amplitude consists in multiplying the signal of the message to transmit by the bearer's signal. The curve of the following Fig. 19 shows the result of the modulation (the frequency of the bearer's signal is fixed by N = 1200 and k = 3, the frequency of information is adopted for N = 120 and k = 8).

One used, also the recurrent Eq. 3 to the digital technique of transmission with frequency modulation. for this purpose, one has replaced in this equation, the coefficient k by a sinusoidal signal given by the same shape of equation:

$$y_k = 2\cos(\alpha)\, y_{k-1} - y_{k-2}$$

In this case, the curve of the following Fig. 20 illustrates the result of modulation.

CONCLUSION

In this study, some methods of frequency synthesis in analog and digital forms are presented. The PLL's technique has been successively used in the synthesizers design. Two techniques of frequency synthesis have been treated such has the fractional-N and the sigma-delta fractional-N PLL's which are frequently used with wireless products and digital signal processors. In these techniques, the synthesized frequency has a stability and accuracy as well as the crystal reference frequency. We have also conceived and proposed an implementation on DSP of the recursive equation, permitting to generate the function of a digital oscillator as a digital frequency synthesizer. The desired frequency is gotten while acting merely on the choice of the parameter "α", where the amplitude is fixed by the initial conditions. The implementation has given interesting results for future extensions in the digital transmission area. In the objective of applying this process of frequency synthesis to an intelligent communication protocol assuring the control and the governing of systems from a far way without connections (Wireless technique), it seems interesting to exploit this digital synthesizer in the domain of modern telecommunications.

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