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Design of an Error Tolerance Flip-Flop for Pipeline Architecture for SOC

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Abstract: The study presents a error tolerant Flip-Flop design for pipeline Architecture for SOC. The proposed design uses the Error Detection and Correction (EDC) technique to achieve the goal. The design is applicable to all pipeline architectures. The proposed research uses the pulse generator and metastability detector to design the error tolerant pipeline. Timing failures induce delayed responses at the outputs of combinational logic circuits which leads to timing error. The research proposes the timing dilation correction circuit like after error detection the evaluation time for the logic is automatically extended by a single clock cycle for error correction using correct and valid data stored in each Flip-Flop. The proposed Error Detection and Correction (EDC) circuit is implemented using a pulse generator, D-flipflop, Xor and Latch. The implementation is performed in The power analysis is done through LTSpice tool in PTM 90 nm technology.

Key words: EDCF, flip flop, pipelining, timing errors, error detection and correction

INTRODUCTION

In Literature survey several techniques are presented based on Timing errors an increasing reliability concern in nanometer technology, high complexity and multi voltage/frequency integrated circuits. After that a new technique is proposed on error detection and correction technique is presented, this research is based on a new bit flipping flip-flop. Whenever a timing error is detected, it is corrected by complementing the output of the corresponding flip-flop. The proposed solution is characterized by very low silicon area and power requirements compared to previous design schemes in the open literature. In this study, McPherson (2006) have proposed an existing CMOS materials much closer to theirintrinsic quality cutoff points are Scaled, for improved execution and cost reduction. It requires creators must be exceptionally watchful with: high current densities, voltage overshoots and confined problem areas on the chip, high obligation cycle applications and high warm resistance bundling. Mitra *et al*. (2005), study a noteworthy obstruction to strong framework outline of physical radiation due to Transient errors . A frame work's weakness to such blunders increments in cutting edge advances, making the fuse of successful assurance instruments into chip outlines fundamental. Agarwal *et al*. (2007) proposed the event of a circuit disappointment before blunders really show up in framework information and states are predict by Circuit disappointment forecast. Circuit disappointment expectation is performed amid framework operation by dissecting the information gathered by sensors embedded at different areas inside a chip. This idea of circuit disappointment forecast for a predominant PMOS maturing system instigated by Negative Bias Temperature Instability (NBTI). Makris *et al*. (2004) depends on the thought of way invariance that present an ease simultaneous test strategy for improving the unwavering quality of RTL controller-datapath circuits. The major perception supporting the proposed philosophy is that the intrinsic straight forwardness conduct of RTL segments, commonly used for various leveled disconnected from the net test, renders rich wellsprings of invariance inside of a circuit. Nicolaidis (1999) expanded about working frequencies, geometry contracting and control supply lessening that go with the procedure of profound submicron scaling, influence the dependable operation of profound submicron ICs. The impacts of different commotion sources are happening to incredible concern. Matakias *et al*. (2004) proposed another circuit for simultaneous delicate andtiming blunder recognition in CMOS Ics. The circuit depends on current mode sense speaker topologies to give quick blunder identification times. On the off chance that a blunder has been identified it can be remedied by utilizing a retry cycle. Valadimas *et al*. (2010) proposed a timing error tolerance play an essential configuration parameter in nanometer innovation, rapid and high multifaceted nature coordinated circuits. In this research, a minimal effort, various timing blunder location and adjustment method which depends on another Flip-Flop plan. Samanta *et al*.

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(2008) proposed a nanometer administration; IC planners are battling between huge variety impacts and tight power limitations. The traditional methodology utilizing timing security edge, devours control constantly to prepare for low likelihood timing varieties. Notwithstanding, the blunder revision plan of Razor reasons pipeline slowing down/flushing and along these lines is not favored progressively frameworks or consecutive circuits with criticism circles. W e propose a flexible timing plan which can amend timing blunders without slowing down/flushing pipeline. Choudhury *et al*. (2010) proposed a Raising dynamic variability with innovation scaling has made it crucial to consolidate huge outline time timing edges to guarantee yield and solid operation. This study presents TIMBER, a system for web borrowing so as to time blunder flexibility that covers timing mistakes time from progressive pipeline stages. TIMBER-based mistake covering can recoup timing edges without direction replay or move back backing. Two consecutive circuit components TIMBER flip-lemon and TIMBER hook that actualize blunder concealing in view of time-acquiring are portrayed. Floros *et al*. (2008) proposed a timing disappointments of high intricacy high recurrence circuit outlines, are a genuine worry in nanometer advancements.

In this research, the Time Dilation (TimeD) scan architecture is proposed which is suitable for both simultaneous mistake location/rectification and disconnected from the net testing. The TimeD structural planning offers simultaneous numerous blunder recognition and revision at the little punishment of one clock cycle delay at the typical circuit operation for every mistake remedy. Valadimas *et al*. (2014) proposed a timing mistake resilience is of incredible significance in nanometer innovation incorporated circuits. In this study, the Time Dilation plan strategy is suggested that gives simultaneous mistake location and revision in the field of use furthermore underpins disconnected from the net assembling filter testing. By using another output Flip-Flop, the time dilation strategy is fit to recognize and rectify different blunders at the base punishment of one clock cycle delay. Valadimas *et al*. (2012, 2015) proposed the Fortifying disappointment instruments highlight timing mistakes as a genuine risk in nanometer innovation microchip centers. In this study, an ease and low-power, numerous timing mistake recognition and redress procedure, depend on another flip-failure plan. The proposed and the surely understood Razor methods were connected independently in the configuration of two variants of a 32-bit MIPS chip center utilizing a 90nm CMOS innovation. Nicolaidis (2007) proposed a silicon-based CMOS innovations are quick drawing closer their definitive cutoff points. By drawing nearer these points of confinement, force dispersal, manufacture yield and unwavering quality decline relentlessly making further nanometric scaling progressively troublesome. The study describes the principles of GRAAL (Global Reliability Architecture Approach for Logic), another flaw tolerant building design for rationale outlines, intended to give a worldwide answer for moderating the aforementioned issues. Yu *et al*. (2011) proposed a delicate blunders have been developed as an essential unwavering quality worry of present day ICs. This study actualized a proficient mistake discovery plan in a low power DSP/MCU processor. Our plan accomplishes high blunder identification proficiency at low equipment cost by method for a unique blend of twofold inspecting and lock based-outline into the purported GRAAL structural engineering.

Theoretical background: Timing failures induce delayed responses at the outputs of combinational logic circuits. In case that a delayed response arrives after the triggering edge of the system clock CLK, the corresponding memory element captures an erroneous value and a timing error is generated. The Flip-Flop is modified to operate as a copier of the main Flip-Flop, latching the same data with a exact delay. A XOR gate is used to compare the outputs of the Flip-Flop pair and detect errors in the system Flip-Flop. Three logic gates are used to enable the trapping of error indication signal at the XOR output in the pertinent scan Flip-Flop. This error indication is shifted out using the existing scan path in order to activate system recovery through re-execution. This is the background of the proposed work. But the main drawbacks of this technique are the high area cost and the performance degradation due to the complexity of the main Flip-Flop, usage of control signals and the high penalty in error detection latency despite the reduction of the global routing of error signals due to the reuse of existing scan facilities made the existingmethod disadvantage. Here in this work we propose a modified architecture for pipelining architecture.

MATERIALS AND METHODS

The proposed method uses a architecture where the disadvantages happening in the previous system are rectified. With addition gates but the execution time is saved when error occurs the Time error detection and correction flip flop. The execution process is evaluated based on a execution of data in the pipelining. If any data is found erroneous in the previous designs it will detect but for correction more time will be consumed. In this work once the error is found an alternative logic immediately corrects it by which the execution time will be saved. The structure of the proposed design for the pipelining is given in Fig. 1. The structure consists of a Multiplexer, 2 flip flops, xor gate and suppy-ground units.

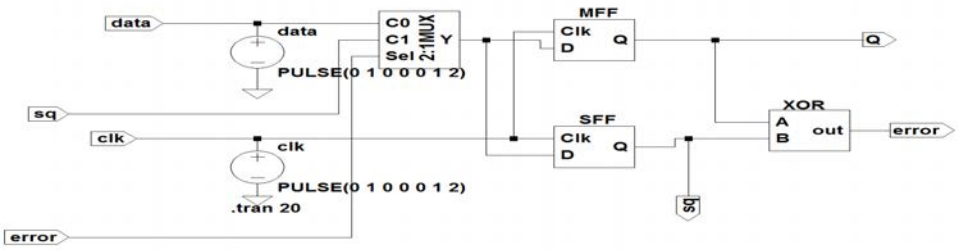

Fig. 1: Schematic diagram of the proposed Flip flop for pipelining Architecture

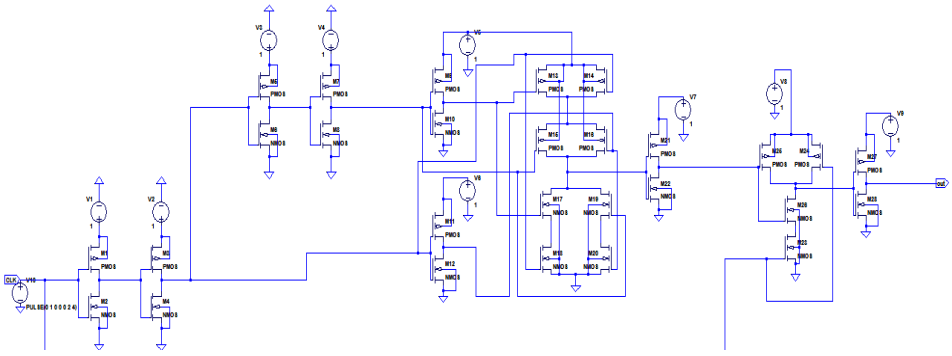

Fig. 2: Schematic diagram of the Pulse generator

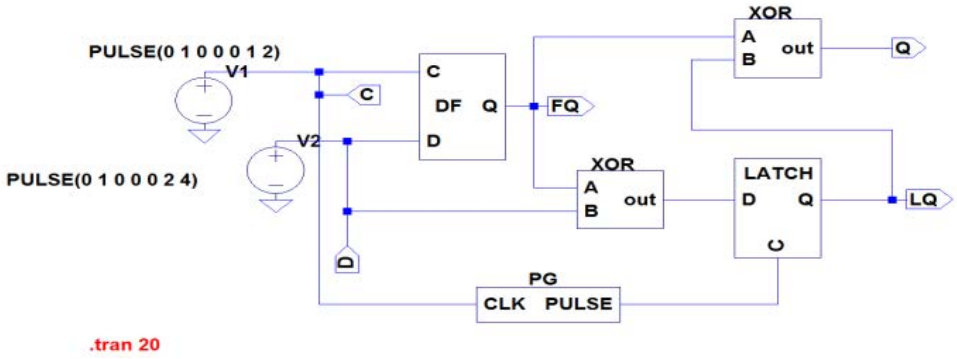

Fig. 3: Schematic diagram of the conventional flip flop

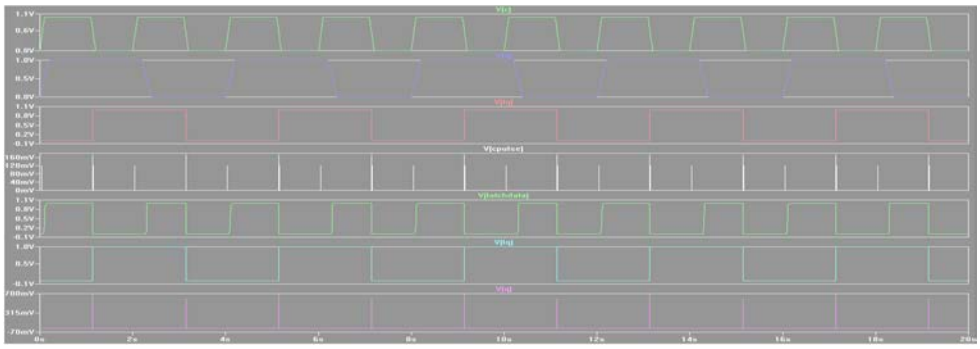

Fig. 4: Simulation output of the conventional EDC flip flop

Table 1: Power analysis

Methods	D-FF	PG	XOR1	XOR2	LATCH	TRIINV	MD
Conventional EDC method	3.0783779e-13	4.922447e-9	3.8882724e-14	3.8882705e-14	3.8621745e-14	-	-
Proposed EDC	4.1638541	9.1807326e-10	3.8883201e-14	3.8883203e-14	3.8621745e-14	0.0024677257	4.1659641

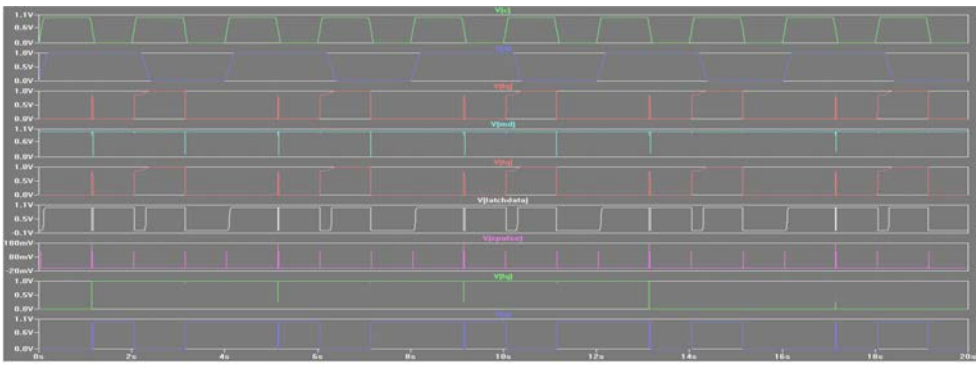

Fig. 5: Simulation output of the Proposed flip flop

RESULTS AND DISCUSSION

The proposed Timing error detection and correction Flip-Flop was designed, implemented and evaluated (Table 1). The flipflop performs the operation using pulse generator, D-flipflop, XOR and Latch. The D-flipflop output is given to the 2 XOR gates and that output is given to the latch makes it possible to estimate the expected value of results. Figure 2 shows the pulse generator schematic view.

Figure 3-5 shows the schematic view and simulation output of the conventional Error detection and correction flip flop. The proposed flip flop power analysis is done through LTSpice tool in PTM 90nm technology.

CONCLUSION

Timing error tolerance is of great importance in nanometer technology integrated circuits. In this work a new architecture for to eliminate Time Dilation is proposed that provides concurrent error detection and correction. The new design reduces the silicon area overhead and the power consumption are substantially reduced, as compared to the existing design approach. The proposed error detection and correction technique is based on the bit-flipping flip-flop concept. The TEDC flip flop is implemented and the results are been observed. The power analysis is done for the various blocks implemented like pulse generator, D-flip flop, XOR and Latch. The simulation outputs for the conventional and proposed EDC flip flop are presented. The implementation and power analysis is done through LTSpice tool in PTM 90 nm technology.

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