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Integration of Sigma-Delta ADC with Sinc Filter on FPGA

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Abstract: This study presents the architecture of FPGA-based Sigma-Delta ADC (SD ADC) utilizing higher integration of noise-shaper modulator and a sinc filter. The noise-shaper modulator employed the Low Voltage Differential Signaling (LVDS) as a comparator for maximum integration. Shaping the quantization noise to higher frequencies is achieved by placing the integrator block of Sigma-Delta Modulator (SDM) across the analog input signal results in lowering the noise level in the bandwidth of interested. Therefore, higher Signal to Noise and Distortion (SINAD) and Effective Number of Bits (ENOB) is able to be achieved with less filter and decimation stage complexity. Sinc filter is chosen as hardware efficient digital filter and decimation stage. Both the integrated noise shaper modulator and the sinc filter on the FPGA results in higher SINAD and ENOB. The architecture is designed and simulated on Quartus II. The SD ADC is implemented on Altera DE-I Cyclone II FPGA board for 8 bit resolution. The results achieved 45.14 peak SINAD and 7.21 bits peak ENOB over a 10 kHz signal bandwidth.

Key words: Integrated sigma-delta ADC, sinc filter, FPGA, resolution, bandwidth

INTRODUCTION

Implementing SD A/D converters on FPGA have received increased attention (Palagiri *et al*., 2012; Uchagaonkar *et al*., 2012; Mihalov and Stopjakova, 2011; Lattice Semiconductor Corp., 2015; Syahril and Isa, 2010; Sousa *et al*., 2004). Compared to different types of data converter capability to be integrated on FPGA for n bit resolution the flash ADC requires $2^{(n-1)}$ comparators that would occupy a considerable number of LVDS pins as 1 bit comparator. Successive approximation ADC implementation on FPGA is involved with n bit off-chip DAC feedback loop in the structure which diminishes the integration. Moreover, pipeline ADC FPGA-based structure demands for n bit quantizer which needs more hardware requirements. The advantage of sigma-delta ADC over other types of ADC as the best choice for FPGA implementation is because it is less sensitive to analog circuit imperfections (De la Rosa, 2011; Abbiati *et al*., 2004; Ritoniemi *et al*., 1990). Though the advantages of sigma-delta A/D converters integration on digital board are widely recognized. However, the feasibility of 1st order Sigma-Delta Modulator (SDM) implementation on FPGA is proved in limited previous works utilizing one, single-bit comparator and DAC feedback loop and sampling element. For example, in some previous published works the integrator of SDM was connected to negative terminal of LVDS and the input analog voltage was connected directly to positive terminal of LVDS. This architecture of SDM named as non-noise shaper SDM that does not shape the quantization noise to higher frequencies. Thus, in order to compensate the extra quantization noise inside the desired bandwidth the multi-stages and/or high order FIR filter and decimation stages was utilized (Palagiri *et al*., 2012; Sousa *et al*., 2004). Also, the maximum integration of SDM was not achieved due to employing off-chip comparator instead of on-board LVDS as 1 bit quantizer by Uchagaonkar *et al*. (2012) and Lattice Semiconductor Corp. (2015). On the other hand, some researches on this field only focused on SDM part integration with no realization of digital filter stage while some others only focused on digital filter and decimation part for SD ADC (Singh *et al*., 2013; Maity and Das, 2012; Mihalov and Stopjakova, 2011; Syahril and Isa, 2010).

This study introduces the integrated noise-shaper modulator by placing the integrator block of SDM across the analog input signal and applied its maximum integration by using LVDS structure as comparator. Noise-shaper modulator reduces the noise level in the desired bandwidth. Thus, higher SNDR and ENOB achieved with less digital filter complexity.

In this study, the full structure of SD ADC is investigated with 1st order integrated noise-shaper sigma- delta modulator and second order sinc filter as single stage hardware efficient digital filter. This architecture is different from previous designs which used a non-noise shaper modulator with the multi-stage, complex digital filter to compensate the quantization noise in the interested bandwidth. The main concern is to achieve high ENOB while using hardware efficient digital filter block and apply maximum integration of overall design. The output signal is evaluated for its dynamic parameters.

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SYSTEM-LEVEL DESIGN

The system-level design process starts from the design of the loop integrator in SDM. By selecting the right topology for SDM and taking advantages of LVDS input buffer the maximum integration with noise shaper modulator achieved. The filter and decimation stage is implemented with the logic resources available in FPGA.

Modulator topology: Basic SDM structure as shown in Fig. 1, consists of 4 block diagrams. All blocks are replaced by their digital counterparts excluding the integrator block. The integrator structure has used the minimum off-chip components which is two passive resistors and one capacitor constructing loop filter. Despite from previous works using discrete external comparator (Lattice Semiconductor Corp., 2015; Miao *et al*., 2008) higher integration of SD ADC optimized by utilizing on-board LVDS input buffer as comparator for noise-shaper SDM. The important consideration is that the time-constant, designed large enough to adequately filter the PWM stream but not so large to dampen response time.

The output of LVDS sampled at 50 MHz clock frequency utilizing D flip-flop as sampling element. The sampling element produces the PWM bitstream filter/decimation stage and DAC feedback loop. The feedback loop transmits the PWM signal to a conventional I/O pin of FPGA that functioning as 1 bit DAC to provide the analog conversion of PWM signal for off-chip integrator. The SDM structure stabilized easier when realizing single-bit quantizer and single-bit DAC feedback to avoid non-linearity problem. The main function of SDM is to perform two signal processing techniques, noise shaping and oversampling. Over Sampling Ratio (OSR) is defined as:

$$OSR = \frac{f_s}{2f_{BW}} \quad (1)$$

Where:
f_s = The clock frequency of sampling element
f_{BW} = The bandwidth frequency of input signal

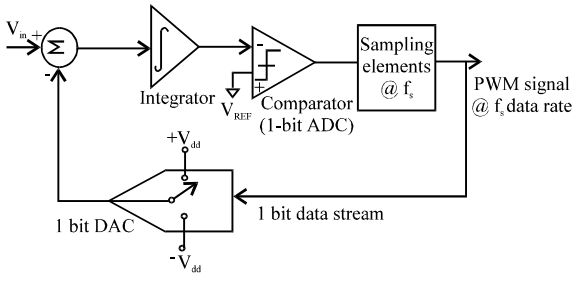

Fig. 1: Basic sigma-delta modulator architecture

Oversampling spreads the sampling noise power across the frequency spectrum; the remaining noise in interested bandwidth is a severe problem in SDM, especially for high resolution designs. In this design, the maximum integration of noise-shaper modulator shaped the in-band quantization noise to higher frequencies for further digital filtering.

CIC digital filter and decimation stage: Digital filter and decimation stage applied after SDM block to extract information from PWM signal, reduce the data rate from 50 MHz to a more useful value and average the 1 bit data stream to improve the ADC resolution. In order to meet hardware efficient design for digital filter and decimation stage, sinc filter is chosen as it is multiplierless digital filter. The transfer function of sinc filter expressed as:

$$H(z) = \frac{1}{DR} \cdot \left(\frac{1-z^{-DR}}{1-z^{-1}} \right)^K \quad (2)$$

Where:
DR = Decimation Rate
K = The order of sinc filter

Decimation rate defines the value of output sample rate. Several designs for sinc filter with various values for order and decimation rate is carried out for higher SNR at the output.

There is always a trade-off between the resolution and output sample rate as well as the FPGA resources and quality of results. The experiments show the output resolution of proposed SD ADC could not exceed 3 bit at 24.41 ksp while the order of sinc filter is one. Applying sinc filter order 3, the actual number of bit achieves to 16 bit at 195.3 ksp. However, for higher resolution of 12 bit and above more complex filter requirement is needed. Increasing the output sample rate to achieve moderate resolution of 8 bit, involved a considerable amount of quantization noise at the circuit operation. Moreover, higher order of sinc filter, 4 and above has not met the required resolution and sample rate at the output. Thereby, designing sinc filter order 2 with DR = 256 eventuate to 8 bit at 195.3 ksp with high SNR at the output while utilizing only one stage digital filter. The digital filter and decimation stage is programmed using Verilog code in Altera Quartus II Software.

SIMULATION RESULTS

Figure 2 illustrates the architecture of integrated SD ADC on FPGA. The architecture consists of sigma-delta modulator and digital filter and decimation stage. The quantization error is the difference between analog input signal and single-bit DAC. The parameters of SDM were designed to alleviate the quantization noise inside the interested bandwidth.

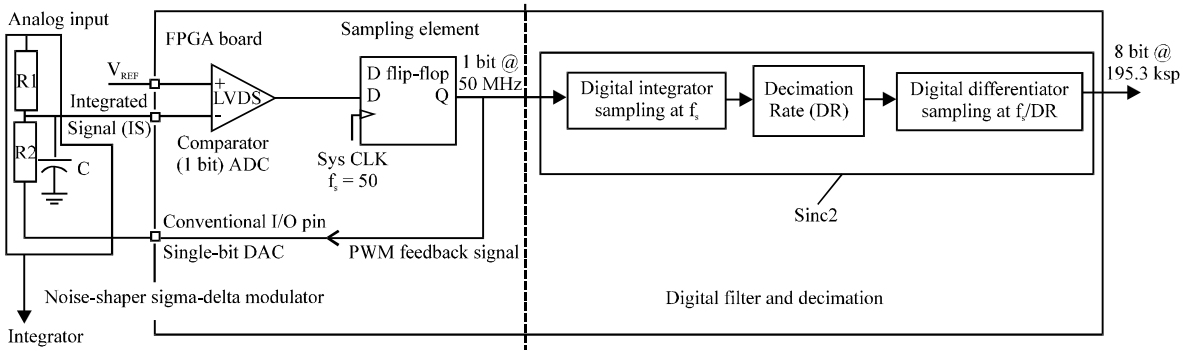

Fig. 2: Proposed sigma-delta ADC architecture integrated on FPGA

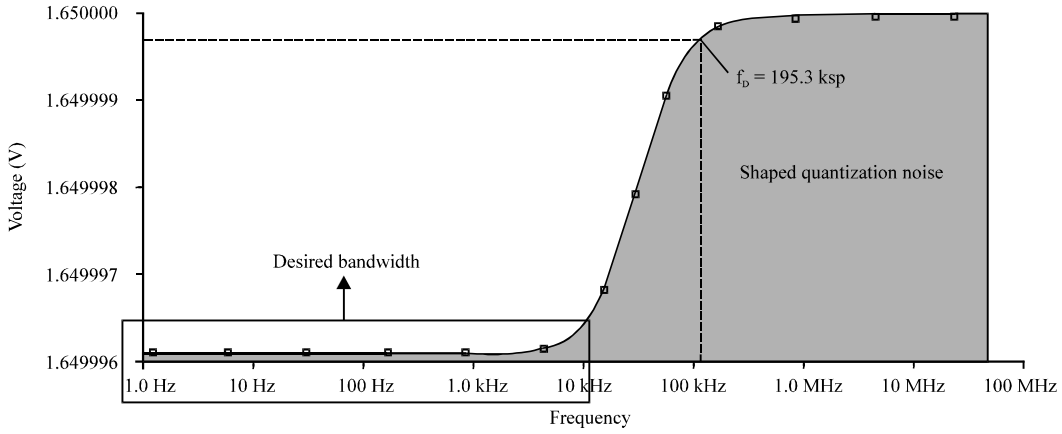

Fig. 3: Noise shaping of sigma-delta modulator

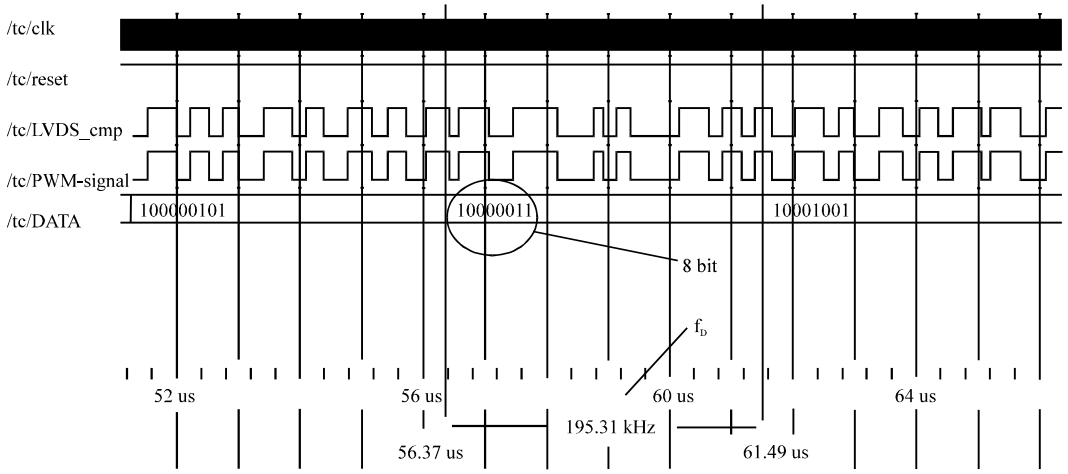

Fig. 4: Simulation of proposed sinc filter functioning

The simulation result for noise shaping is as shown in Fig. 3. Most of the quantization noise in low frequencies up to 10 kHz has moved to higher frequencies. The proposed SDM structure with its maximum integration performs noise shaping from desired bandwidth which results to improve SINAD and ENOB at the output of SD ADC in comparison with non-noise shaping modulator.

The quantization noise which is involved in the interested bandwidth is shown in Fig. 3. The reduction of

quantization noise in the signal-band improves SINAD and ENOB. Digital filter and decimation stage defines the output resolution and data rate. SD ADCs use other filters in conjunction with sinc filters as part of a process called two-stage decimation. However, industrial SD ADCs usually use only the sinc filter (Baker, 2011). The modelsim simulation of sinc filter order 2 with DR = 256 at sampling frequency is shown in Fig. 4. Two transitions of output data is captured it shows that the output data is 8 bit at 195.31 ksp.

SIGMA-DELTA ADC FPGA IMPLEMENTATION

The proposed SD ADC has been implemented in FPGA with the input voltage range of (0-3.3V) and input frequency range of (23 Hz-10 kHz). The multi-bit output data of the chip was passed through R-2R DAC to display the analog conversion of digitized signal on oscilloscope. Furthermore, the FFT graph with 8192 points analyzes the dynamic performance of SD ADC. A sinusoidal analog signal of a given frequency was generated and applied to the input of the converter. The evaluation held on dynamic parameters of integrated ADC. Figure 5 depicts the input waveform and output waveform at 23 Hz. As seen there is 180^ phase shift between input and output waveforms due to the connection of analog input signal through the negative pair of LVDS.

Digital analysis on 8 bit output data is shown in Fig. 6. Dynamic analysis of data shows that the output signal reconstructed at 23 Hz at 195.3 ksp as expected and achieves to 7.21 bits ENOB and 45.14 dB SINAD. Figure 7 reveals that by increasing the input frequency to 10 kHz the output signal still retains its sinusoidal properties. The phase shift measured as 108.12^.

Similarly, the digital analysis on output data is shown in Fig. 8. The FFT graph with 8192 points presents the harmonics of output signal. The output signal reconstructed at 10 kHz at 195.3 ksp as expected and achieves to 6.52 bits ENOB and 41.00 dB SINAD. The SINAD and ENOB distribution from 23 Hz to 10 kHz illustrates in Fig. 9. The best value was found at 23 Hz.

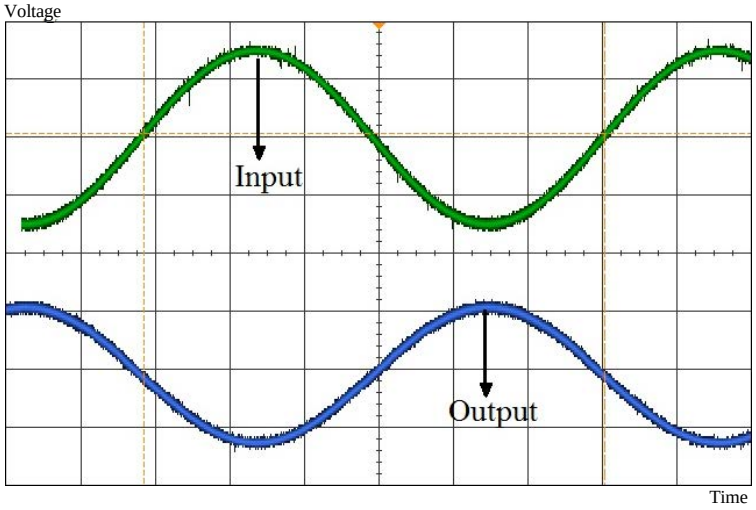

Fig. 5: SD ADC input and output at f_{in} = 23 Hz (no sinc2 correction is applied)

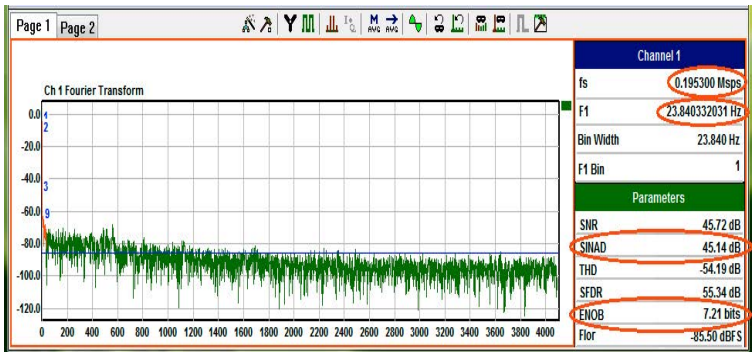

Fig. 6: Results of data analysis for low frequency option, f_{in} = 23 Hz

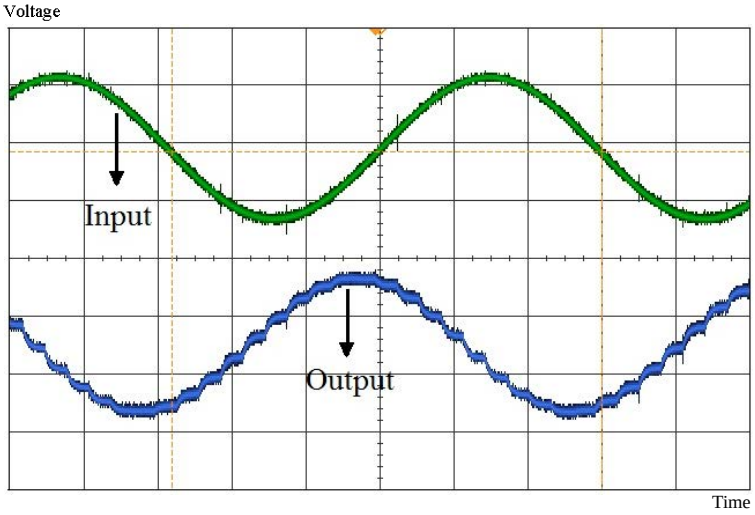

Fig. 7: SD ADC input and output at f_{in} = 10 kHz (no sinc2 correction is applied)

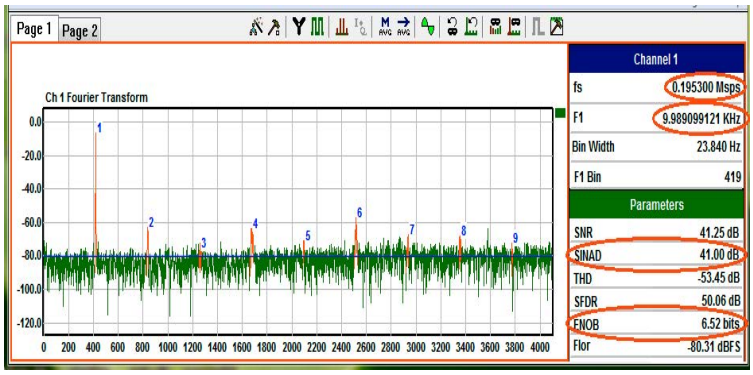

Fig. 8: Results of data analysis for low frequency option, f_{in} = 10 kHz

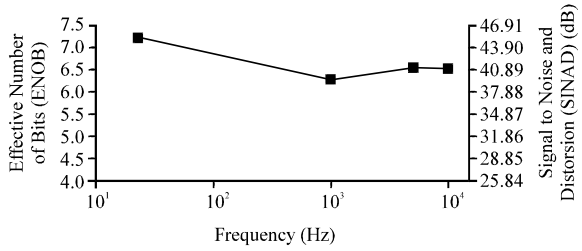

Fig. 9: Measured ENOB and SINAD distribution for implemented SD ADC

CONCLUSION

Integration of SD ADC into Altera Cyclon II DE 1 FPGA has accomplished using hardware description language Verilog. First order noise-shaper modulator shaped the quantization noise to higher frequencies. Hardware efficient sinc2 filter following the modulator block with DR = 256 were programmed on FPGA. It converts 1 bit at 50 MHz to 8 bit at 195.3 ksp. The experimental results prove the feasibility of the proposed SD ADC over 10 kHz frequency ranges where the ENOB and SINAD achieve to values higher than 6.28 bits and 39.74 dB, respectively. Higher order SDM shapes even more quantization noise to higher frequencies which improves ENOB but it will decrease the integration.

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