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Low Drop Out (LDO) Regulator using a High Precision Band Gap Reference (BGR)

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Abstract: This study presents the design criteria of Low Drop Out (LDO) regulator using a high precision Band Gap Reference (BGR) which make the system independent of PVT variations. The inspiration behind the study of LDO regulators is driven by the increasing demand for higher performance power supply circuits. The BGR provides a reference voltage of 0.9 V, that can be vary according to the requirements. The designed LDO will provide an output voltage of 1.8 V with ±3% variation across the PVT variations. The study further illustrates the analysis and the results relevant to the LDOs and BGR using 55 nm CMOS technology.

Key words: BGR, LDOs, error amplifier, pass transistor, folded cascode amplifier, CMOS

INTRODUCTION

In analog circuits, voltage and current regulators are used extensively. The reference voltage or current are dc quantities that are independent of process, voltage and temperature. Voltage regulators are used to maintain a constant output voltage which is independent of all the variations around it. There are two types of regulators, switching regulators and linear regulators. In modern IC's linear regulators are preferable over switching regulators even though they have high efficiency compared to linear regulators (Widlar, 1971; Lu *et al*., 2014). That is because of the less complexity, small size, low noise and low cost of linear regulators. Switching regulators are highly efficient able to handle high input voltage range and readily available as modular chips which are very compact and reliable. Isolated and non-isolated switching dividers are available. On the other hand linear regulators are able to powering low powered devices. Apart from that they are easy to use, simple, cheap and small in size.

Low drop out regulator is a dc linear regulator whose output voltage is less than the input voltage. LDO is particularly used to provide a precise power supply voltage which will eliminate the effects of input supply ripples. The advantages of LDO include low production cost, high PSR and easy integration have achieved considerable attention in the mobile battery-operated systems. The main advantage of LDO is it can regulate the output voltage even when the input voltage is more close to the output voltage (Okuma *et al*., 2010). The LDO mainly consist of three components. A reference voltage generator an error amplifier and a pass device. BGR is used as a reference voltage generator which will generate a reference voltage that is independent of PVT variations. The reference voltage will be compared with the feedback voltage which is generated from the output voltage using a resistor divider circuit. The comparison is did using high gain error amplifier, through this the regulation will happen. Here in this study, the design of a low drop out regulator is described with a high precise BGR. The output voltage of BGR only has a 4.93% of variation across the PVT. The architecture that is used for the BGR make the voltage high precise and programmable.

MATERIALS AND METHODS

Proposed LDO architecture: The block diagram of the proposed LDO is shown in Fig. 1. Mainly it consist of three parts BGR, error amplifier and a pass device. The BGR is used to provide the reference voltage to the error amplifier. The error amplifier will regulate the output

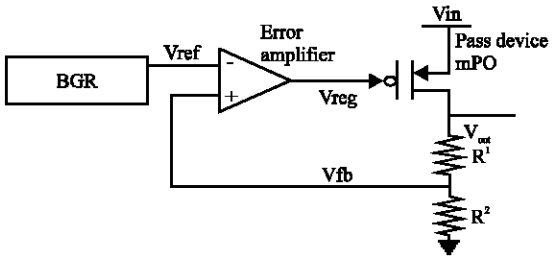

Fig. 1: Proposed LDO block diagram

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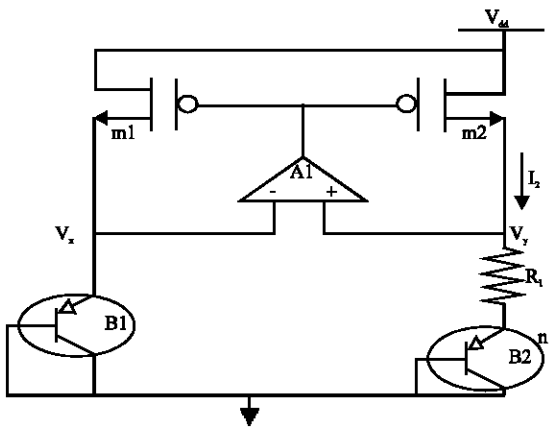

Fig. 2: Conventional BGR circuit

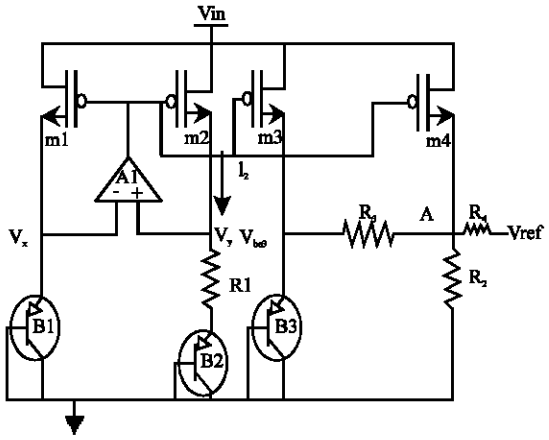

Fig. 3: Modified BGR circuit

voltage through the negative feedback. If the output voltage is increased due to some PVT variations, then V_{fb} and V_{reg} will also increase, that will reduce the current through the pass device as a result V_{out} will regulate to the required value. The same kind of regulation will happen whenever the V_{out} decreases. The voltage drop across the pass device is called drop out voltage or the drop out voltage is simply the difference between the input and output voltages (Behzad, 2001; Leung and Mok, 2003; Kim and Lee, 2013; Srinivasan *et al*., 2008; Gray and Meyer, 1993).

BGR: BGR generates a reference voltage which is independent of PVT variations. BGR is a temperature independent voltage or current reference circuit which provides a constant voltage regardless of PVT variations and circuit loading from a device (Buck *et al*., 2000). Figure 2 and 3 shows the basic BGR architecture:

$$V_x = V_y \text{ (Op-amp A1 will ensure this)} \quad (1)$$

To ensure this condition the op-amp should need a gain of at least 60 dB (Purushothaman, 2016; Sahoo and Razavi, 2013). Equation 1 can be written as follows:

$$V_{be1} = R_1 \times I_2 + V_{be2} \quad (2)$$

$$R_1 \times I_2 = V_{be1} - V_{be2} = \Delta V_{be} = V_t \ln(n) \quad (3)$$

where n is the number of BJT's used in B_2. It is proved that in a BJT, ΔV_{be} has positive temperature coefficient and V_{be} has negative temperature coefficient from Eq. 3:

$$V_y = R_1 \times I_2 + V_{be2} = V_t \ln(n) + V_{be2} \quad (4)$$

Hence, V_y is independent of temperature variations. The problem with this architecture is the non-programmability of the output. For example, at room temperature with zero temperature coefficient:

$$V_y = V_{be2} + 17.2 \times V_t = 1.25\,V \quad (5)$$

To make the output voltage programmable, Fig. 3 showing an architecture which makes the output voltage programmable. In this architecture, by applying KCL at the node A ($V_A = V_{ref}$):

$$I_2 = \frac{V_t \ln(n)}{R_1} = \frac{V_{ref} - V_{be3}}{R_3} + \frac{V_{ref}}{R_2} \quad (6)$$

$$V_{ref} = \left(\frac{V_t \ln(n)}{R_1} + \frac{V_{be3}}{R_\uparrow} \right) (R_2 // R_3) \quad (7)$$

First term has the positive temperature coefficient and second term has the negative temperature coefficient as a result V_{ref} is independent of temperature variations.

Error amplifier: Op-amp with a negative feedback is used as an error amplifier. A differential cascode circuit shown in Fig. 4 can be used as an error amplifier but the problem with this circuit is less output swing, voltage headroom and also the gain that can give is maximum 50 dB. The gain of this circuit is given by:

$$\text{Gain} = g_{m1} \times (g_{m4} r_{02} r_{04} // g_{m6} r_{06} r_{08}) \quad (8)$$

For increasing g_{m1}, we will increase the current and that will reduce the resistance so, the gain will not increase. Using the folded cascode shown in Fig. 5, We

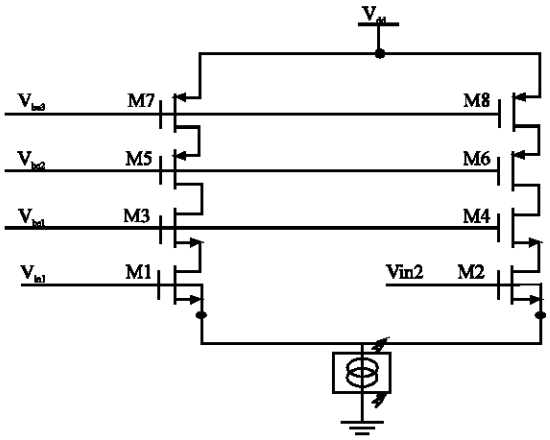

Fig. 4: Differential cascode

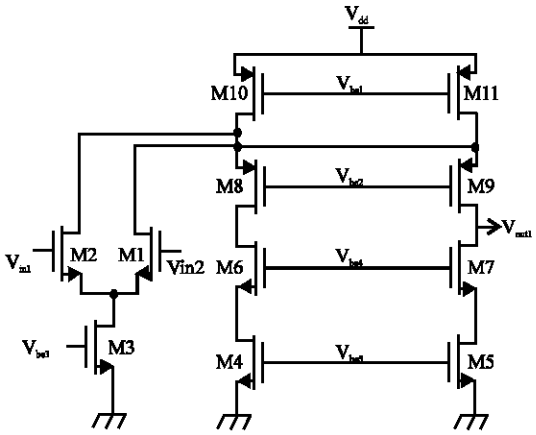

Fig. 5: Differential folded cascode circuit

will get independent control on both g_{m1} and resistance and the voltage swing will also get improved. For this architecture gain is given by:

$$\text{Gain} = g_{m1} \times \left(g_{m9} r_{09} r_{011} // g m_7 r_{07} r_{05} \right) \quad (9)$$

Here, it is possible to independently control both the output resistance and the g_{m1} as a result we can increase the gain as per our requirement. The output of the error amplifier is given to pass transistor as bias to it. Through that the control will happened.

RESULTS AND DISCUSSION

The LDO is designed with an output voltage of 1.8 V using the high precision programmable BGR. The described circuit is implemented and simulated in 55 nm cmos technology model. The result is checked across process corner (SS, FF), temperature (-40 to 125) and supply voltage (10% variation in V_{dd}). Results that will shows the accuracy of the system is shown in below sections.

Table 1: Phase margin of BGR-tabulated results acros corner

Process corners	Resistance variations	BJT variations	V_{dd}	Phase margin
FET_ssp_pre	Res_max	beta_min	1.98	56.37
FET_ffp_pre	Res_max	beta_min	1.98	56.37
FET_ssp_pre	Res_max	bata_min	1.62	62.10
FET_ffp_pre	Res_max	beta_min	1.62	62.10
Nom	nom	nom	1.80	63.14
FET_ssp_pre	Res_min	beta_max	1.98	66.83
FET_ffp_pre	Res_min	beta_max	1.98	66.83
FET_ssp_pre	Res_min	beta_max	1.62	70.59
FET_ffp_pre	Res_min	beta_max	1.62	70.59
Max:PM				70.59
Max:PM				56.37

Table 2: Output regulated voltage of LDO-tabulted results across corner

Process variations	Resistance variations	Temperature	V_{dd}	V_{out}	Percentage of variations
FET_ffp_pre	Res_max	125	3.24	1.750	2.777777778
FET_ssp_pre	Res_max	125	3.24	1.750	2.777777778
FET_ffp_pre	Res_max	125	3.96	1.766	1.888888889
FET_ssp_pre	Res_max	125	3.96	1.766	1.888888889
FET_ssp_pre	Res_min	-40	3.24	1.770	1.666666667
FET_ssp_pre	Res_min	125	3.96	1.787	0.722222222
FET_tt_pre	Res_nom	30	3.60	1.803	0.166666667
FET_ssp_pre	Res_min	-40	3.96	1.809	0.500000000
FET_ffp_pre	Res_min	-40	3.24	1.811	0.611111111
FET_ffp_pre	Res_min	-40	3.96	1.822	1.222222222
FET_ffp_pre	Res_max	-40	3.96	1.826	1.444444444
FET_ssp_pre	Res_max	-40	3.96	1.826	1.444444444
FET_ffp_pre	Res_min	125	3.24	1.827	1.500000000
FET_ffp_pre	Res_max	-40	3.24	1.831	1.722222222
FET_ssp_pre	Res_max	-40	3.24	1.831	1.722222222
FET_ffp_pre	Res_min	125	3.96	1.831	1.722222222
FET_ssp_pre	Res_min	125	3.24	1.841	2.277777778
Max. percentage of variation					2.777777778

BGR results: The BGR is designed with a reference voltage of 0.9 V. The reference voltage of the BGR only has variation of 1.79 mV across the temperature in typical corner. The voltage can be tuned to any value using the resistances at the output side. Figure 6 and 7 show the results of BGR voltage at typical and across corner accordingly. Table shown in Fig. 8 gives the stability of the system. The system is stable across the corner with a minimum phase margin of 56°.

Monte-Carlo simulation on the BGR reference voltage gives a standard deviation of 7.00305 m. Table 1 shows the graph of Monte-Carlo simulation.

LDO results: The designed LDO output voltage only has a 2.7% variation across the corner and the entire system is stable across the PVT with a minimum phase margin of 81°. Figure 8 and Table 1-3 show tabulated results of output voltage and stability across PVT.

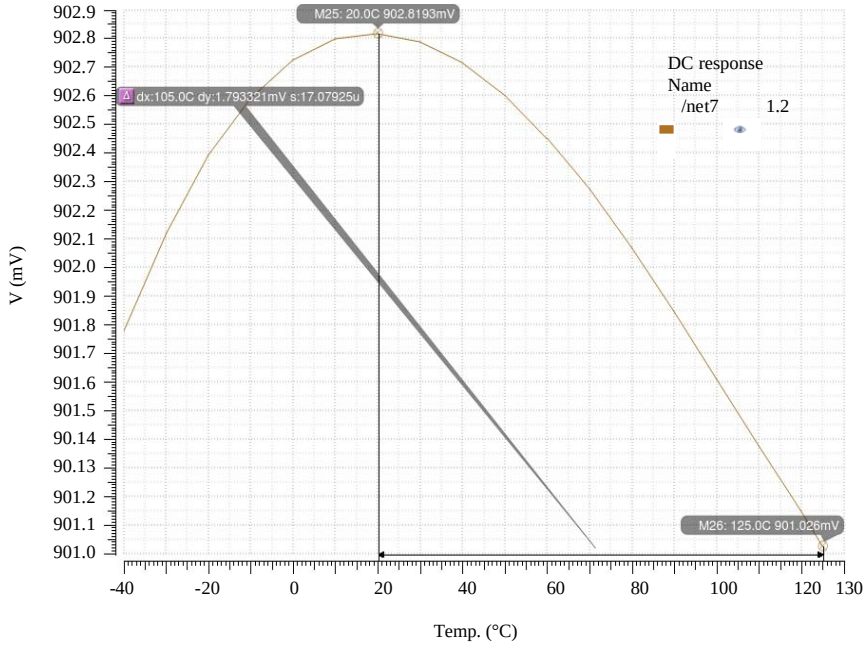

Fig. 6: Output reference voltage of BGR across temperature in typical corner

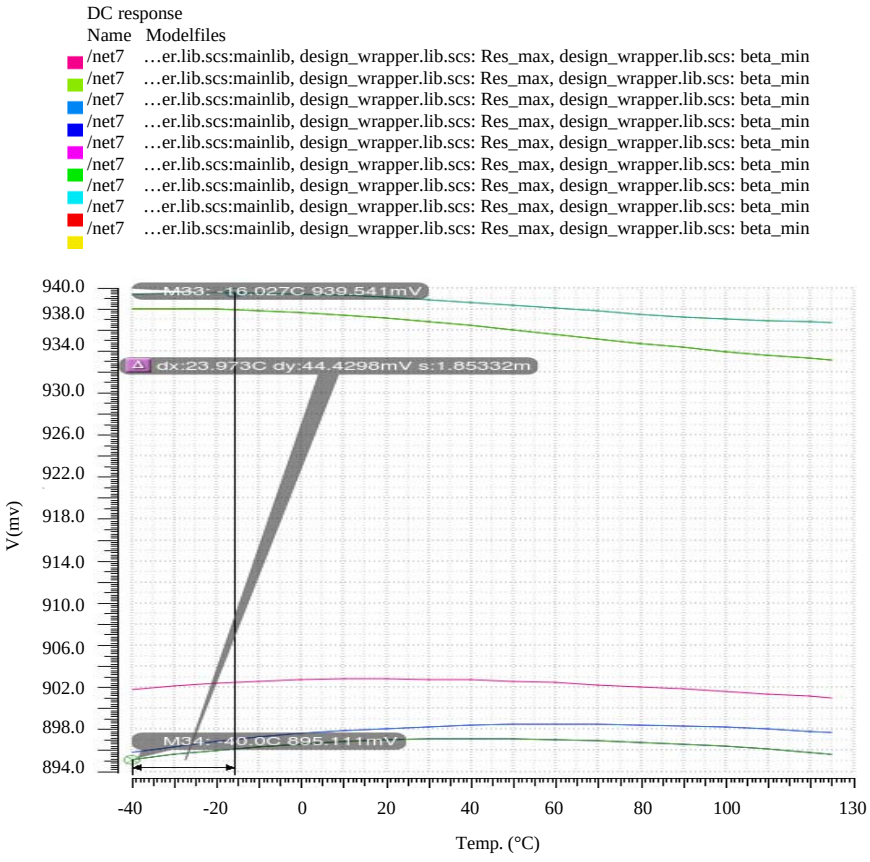

Fig. 7: Output reference voltage of BGR across temperature in across corner

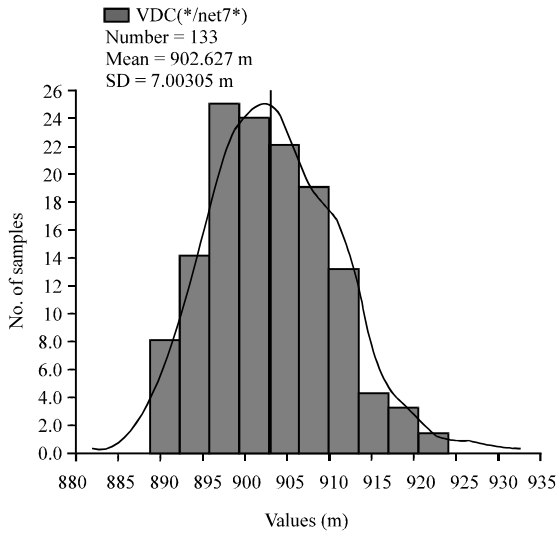

Fig. 8: Monte Carlo simulation result

Table 3: Phase margin of LDO-tabulated results across corner

Process variations	Resistance variations	Temperature (°C)	V_{dd} (V)	Phase margin (degree)
FET_ffp_pre	Res_min	-40	3.24	81.76
FET_ssp_pre	Res_min	-40	3.24	81.76
FET_ffp_pre	Res_min	-40	3.96	84.14
FET_ssp_pre	Res_min	-40	3.96	84.14
FET_ffp_pre	Res_max	-40	3.24	85.84
FET_ssp_pre	Res_max	-40	3.24	85.84
FET_tt_pre	Res_nom	30	3.60	87.79
FET_ffp_pre	Res_max	125	3.24	90.45
FET_ffp_pre	Res_max	125	3.24	90.45
FET_ffp_pre	Res_max	125	3.96	93.80
FET_ssp_pre	Res_max	125	3.96	93.80
FET_ffp_pre	Res_max	-40	3.96	94.35
FET_ssp_pre	Res_max	-40	3.96	94.35
FET_ffp_pre	Res_min	125	3.24	97.72
FET_ssp_pre	Res_min	125	3.24	97.72
FET_ffp_pre	Res_min	125	3.96	106
FET_ssp_pre	Res_min	125	3.96	106
Max. phase margin				106
Max. phase margin				81.76

CONCLUSION

In this study, a low drop out regulator using a high precision, programmable BGR having a 1.79 mV variation across temperature in the typical corner is presented. The system is designed and tested in 55 nm cmos technology. The output regulated voltage of 1.8 V is obtained with a variation of 2.7% across PVT with high stability.

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