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Design of 3.1-10.6 GHz Ultra-Wideband Cmos Low Noise Amplifier for Wireless Applications

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Abstract: Two ultra wideband Low Noise Amplifiers (LNAs) are presented. A common source topology is adopted for input stage to achieve wideband input matching while a cascode stage is used as the second stage to provide power gain at high frequencies. The first work is a LNA with resistive shunt feedback. It achieves a maximum power gain of 10.5 dB, a bandwidth of 10 GHz and 8.7 dB minimum noise fiqure. The power consumption is 14.28 mW from a 1.8 V supply. The second work is common source with a reuse pmos current source.

Key words: CMOS, feedback, gain flaness, low noise amplifier, Ultra Wide Band (UWB)

INTRODUCTION

In recent years, the demand for high-speed and high data-rate wireless communication is increasing. Since, the Federal Communications Commission (FCC) released the 7.5 GHz bandwidth of the spectrum range from 3.1-10.6 GHz for ultra wideband in 2002 (Chen *et al*., 2007). As the essential reasons to uwb systems, it provides a low power level (limit to-41.3 dbm/MHz) and high data-rate (up to 480 Mb/s) for wireless communications (Hsu *et al*., 2013). UWB performs excellently for short-range high speed uses such as automotive collision-detection systems, through-wall imaging systems and high speed indoor networking and playes an increasingly important role in Wireless Local Area Network (WLAN) applications (Chen and Liu, 2012). LNA as the first module of UWB receiver has important influence on the sensitivity and dynamic range of the whole receiver system. The amplifier must meet several stringent requirements such as broad-band input matching to minimize the return loss, sufficient gain to suppress the noise of a mixer, low Noise Fiqure (NF) to enhance receiver sensitivity, low power consumption to increase battery life and small die area to reduce the cost (Zhang and Kinget, 2006) many topologies have been presented in LNA designs such as distributed amplifiers (Liao and Liu, 2007; Sung *et al*., 2011) resistive shunt feedback (Reiha and Long, 2007), cascade amplifiers and current reused amplifiers. Resistive feedback is a well-known wide-band technique used in wide-band amplifiers but it is hard to satisfy gain and noise requirements simultaneously. The distributed amplifier can improve gains at higher frequencies and hence can extend the bandwidth. But, it need more inductors and thus consumes more power. Cascode configured UWB LNAs using LC bandpass filter to achieve the broadband input matching have previously been reported (Huang *et al*., 2015). The current reuse amplifier isuseful for high gain and low power dissipation,but the reported wideband is not enough for 3.1-10.6 Ghz application (Kao and Chung, 2008).

MATERIALS AND METHODS

Basic resistive feedback LNA: The most common resistive feedback LNA is shown in Fig. 1a, b gives an improved topology which reuses the PMOS current source to reduce power and noise in short channel process, the input impedance and voltage gain of LNA in Fig. 1b are expressed as:

$$Z_{in} = \frac{r_{on} \| r_{op} + R_f}{1 + \left(g_{Mn} + g_{Mp}\right)\left(r_{on} \| r_{op}\right)}$$

$$A_v = \frac{\left[1 - \left(g_{mn} + g_{mp}\right)R_f\right]\left(r_{on} \| r_{op}\right)}{R_f + r_{on} \| r_{op}}$$

where, g_{mn} and g_{mp}, r_{on} and r_{op} are the transconductance and output resistance of M_n and M_p, respectively. Indeed, stacking both NMOS and PMOS transistors, the overall equivalent transconductance is increased from g_{mn} to $g_{mn}+g_{mp}$ for the same biasing current. Figure 1 is small signal model in Fig. 1, it is assumed that the circuit is connected to a source generator whose the R_S impedance is typically to 50Ω the noise figure of LNA are expressed as:

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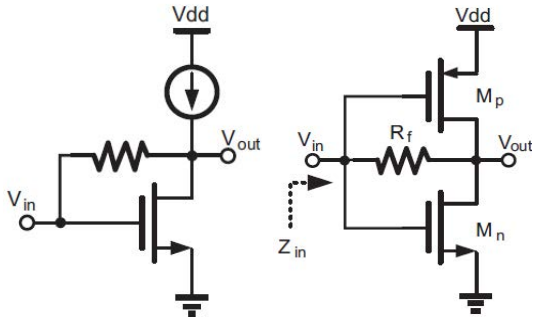

Fig. 1: Traditional resistive-feedback LNA: a) with a current source just for DC-bias and b) with a pmos current source

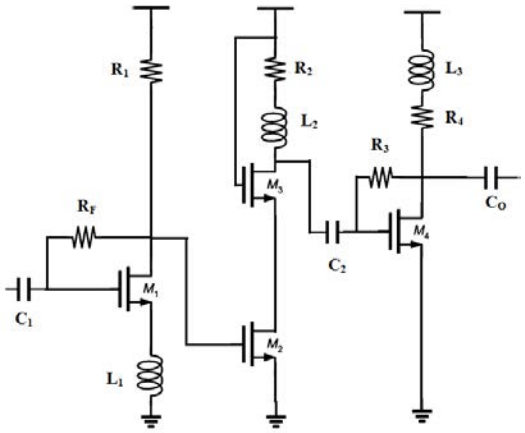

Fig. 2: First UWB LNA

$$NF \approx 1+\frac{2}{3}\frac{1}{\left(g_{mn}+g_{mp}\right)}\left(\frac{1}{R_s}+\frac{R_s}{R_F^2}\right)+$$

$$\frac{2}{3}\left(g_{mn}+g_{mp}\right)R_S\left(\frac{f}{f_T}\right)^2+\frac{R_S}{R_F}$$

RESULTS AND DISCUSSON

Circuit analaysis of LNA

Circuit analaysis of first LNA: The wideband LNA is shown in Fig. 2. It consists of a common source stage, a cascade second stage and an output buffer. The input stage provide the broadband power and noise matching. The input impedence is simplified as:

$$Z_{in}^{1}=g_{m1}\frac{L_{S1}}{C_{GS1}}+sL_{S1}+\frac{1}{SC_{GS1}}$$

where, g_{m1} and C_{gs1} are the transconductance and the gate-to-source capacitance of transistor M_1, respectively Fig. 3. Equation presents a series-RLC network. Where R_p, L_P and C_P can be derived as:

$$R_p=\frac{R^2+\left(\omega L-\frac{1}{\omega C}\right)^2}{R}$$

$$L_p=\frac{R^2+\left(\omega L-\frac{1}{\omega C}\right)^2}{\omega^2 L}$$

$$C_p=\frac{1}{\left(\omega^2 C+\left(R^2-\frac{1}{\omega C}\right)^2\right)}$$

$$R'_F=R_F/(1+A_v)$$

Thus, the input impedance Z_{in} is approximated as:

$$Z_{in}=\left(R'_F\middle|R_p\right)\left\|\left(sL_p\middle\|\frac{1}{SC_p}\right)\right.$$

The simulation effect of RF on the NF is shown in Fig. 4.

Circuit analaysis of second LNA: Figure 5 shows the proposed UWBLNA using a gate inductor. The gate inductor, L_g is connected in series to M_N's gate and forms an LC resonant branch with M_N's gate capacitance C_n. The small signal equivalent circuit of the first stage is illustrated in Fig. 6. Due to the existence of C_{gd} and R_F, the input stage is treated as a bilateral two-port network and the input impedance is influenced by the output impedance of the first stage. According to the small signal model, M_N's equivalent transconductance, G_{M1} is given by:

$$G_{M1}=\frac{g_{M1}}{1-\omega^2 L_g C_{gs1}+j\omega R_{Lg}C_{gs1}}$$

$$=\frac{g_{M1}}{1-\left(\omega/\omega_0\right)^2+J\omega/\omega_0 Q_0}$$

Topology in Fig. 6 can be used to realize similar bandwidth extension by choosing different inductors:

$$G_M=g_p\left(1+\frac{\sqrt{2m}}{1-\omega^2 L_a C_n}\right)$$

$$C_{in}=C_p\left(1+\frac{m}{1-\omega^2 L_a C_n}\right)$$

And:

$$(W/L)_n\ (W/L)_p=m$$

According to C_{in}'s expression when operating frequency is near to ω_0, C_{in} will increase steeply to

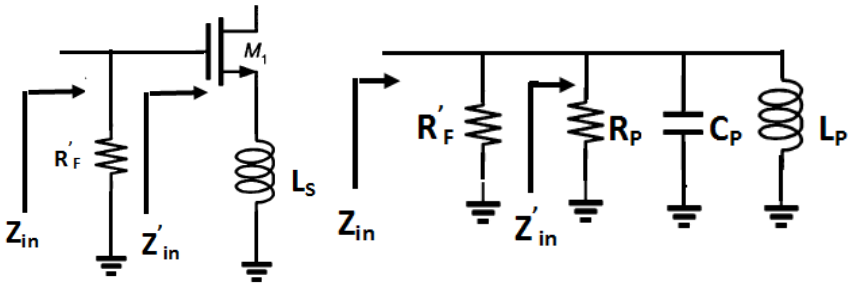

Fig. 3: Miller equivalent circuit

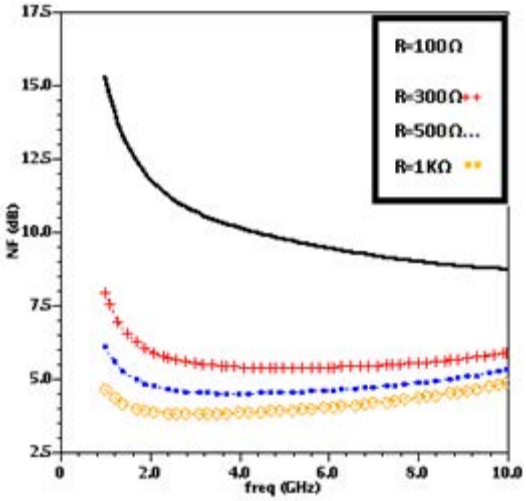

Fig. 4: Effect R_F on NF

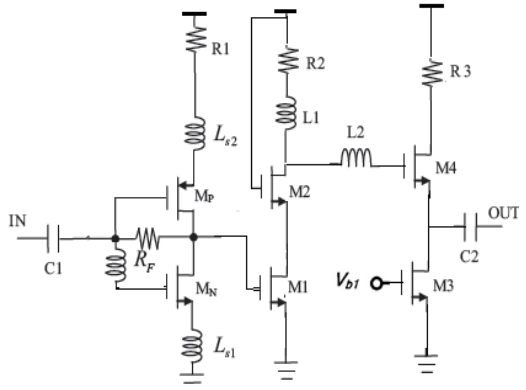

Fig. 5: Proposed ultra wideband LNA

mismatch input. Therefore, suitable resonance frequency of LC series is also important for input matching, not only for gain compensation.

Second stage: The second stage is cascade common-source stage which provides high-frequency

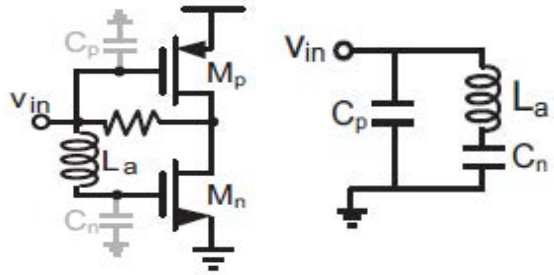

Fig. 6: Gate inductive peaking topology and its equivalent model NMOS peaking

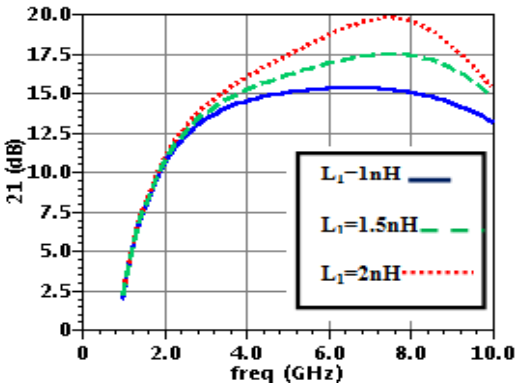

Fig. 7: Effect L_1 on S21

gain and determines higher 3 dB bandwidth of the LNA. The cascade transistor M_4 is used for better isolation, higher frequency response and higher gain. The series peaking inductor L_{D2} can resonate with the total parasitic capacitances C_{D4} at the drain of M_4 and resistor R_{L2} is added to reduce the Q factor of L_{D2} for flat gain. Conventionally, the quality factor of the inductor for LNAs should be as high as possible to achieve high-gain, narrow-band characteristic however, the Q factor of L_{D2} in this design is kept smaller for flat gain of the whole LNA. Hence, an extra resistor R_{D2} of 100 Ω is added to reduce to Q factor. The simulation effect of L_1 on the NF is shown in Fig. 7.

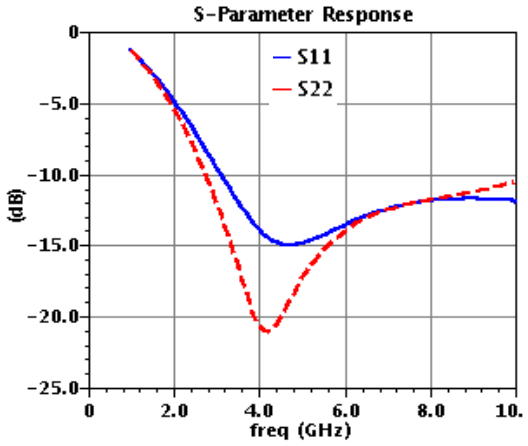

Fig. 8: Input and output return loss first UWB

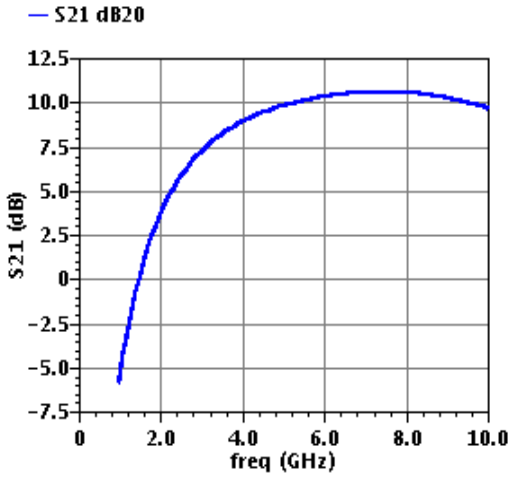

Fig. 9: Power gain first UWB LNA

RESULTS AND DISCUSSION

Output buffer: The buffer is a source follower which has voltage gain of:

$$\frac{V_{out}}{V_b} = \frac{g_{m4}}{1 + g_{m4}R_L}$$

where V_{out} and V_b are the output and input voltage of the buffer shown in Fig. 5. R_L is the load of the buffer and its value is 56 Ω in this study in order to reduce the parasitic capacitance arisen from a larger device, the input device of this buffer must be reduced despite the larger loss occurs. The width and length are set to 56 and 0.18 μm, respectively.

The UWB LNA were simulated in TSMC 0.18 μm CMOS process simulations have been performed using Spectre simulator of cadence. Figure 8 shows the input return loss and output return loss of the first UWB LNA. The simulated inpu and output return loss is below -10 dB. Figure 8 shows input and output return lossof the second UWB LNA, respectively. Figure 9 show the simulated power gain of the first and second UWB LNA. Power gain first LNA is 10.5 dB and power gain second lna is 15.2 dB. The simulation NF of the first lna is illustrated in Fig. 10. The minimum NF is 8.7 dB. S12 of the first LNA and S12 of the second lna shown in Fig. 11-14, respectively.

The simulation NF of the second UWB LNA is illustrated in Fig. 15. The minimum NF is 3.7 dB. The parameters of the first and second UWB LNA's design are listed in Table 1-3 in general, the Fiqure of Merit (FOM) is applied to evaluate performance of LNAs and is defined as:

$$FOM = \frac{\text{Gain max}(dB) \times BW(GHz)}{[F-1] \times Pd(mw)}$$

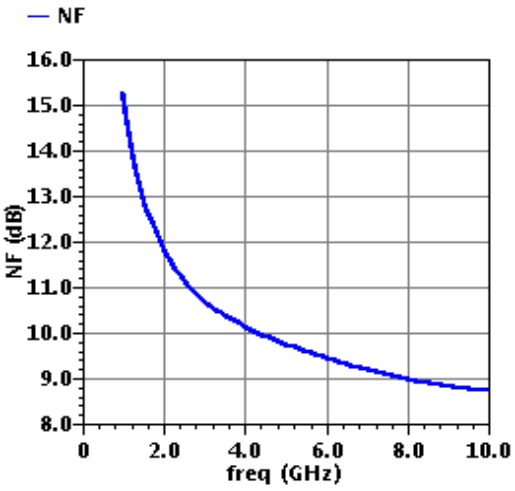

Fig. 10: NF first UWB LNA

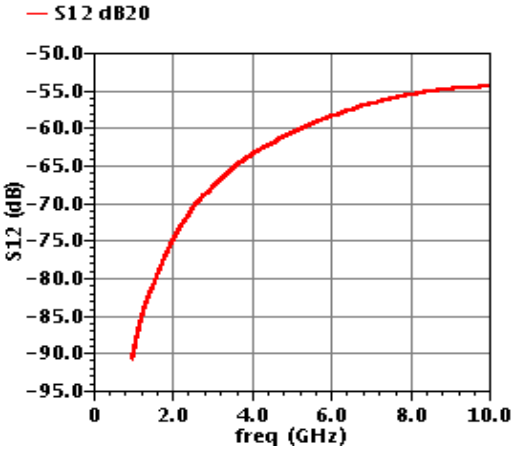

Fig. 11: Simulated S12 of the UWB LNA

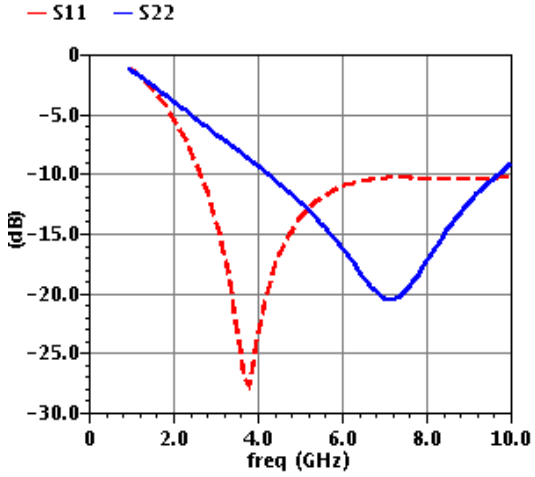

Fig. 12: Input and output return loss second UWB LNA

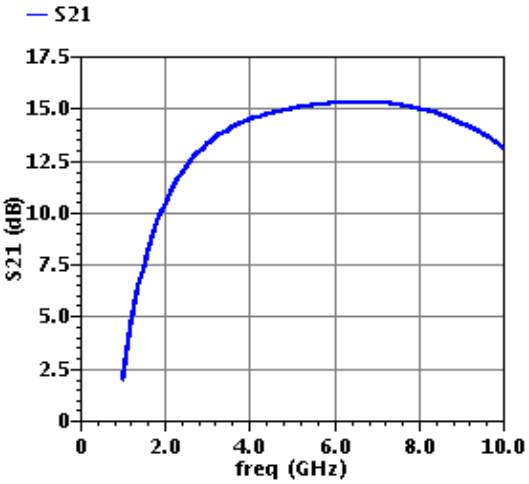

Fig. 13: Power gain of the second UWB LNA

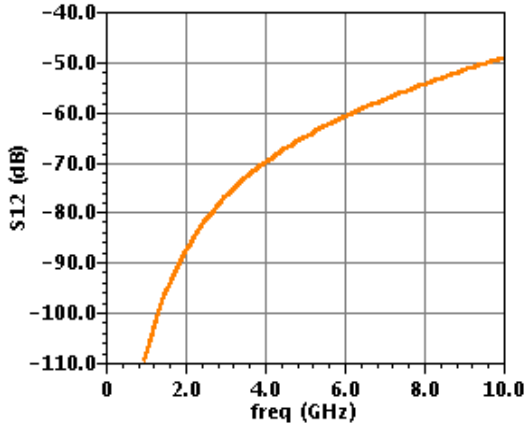

Fig. 14: Simulated S12 of the UWB LNA

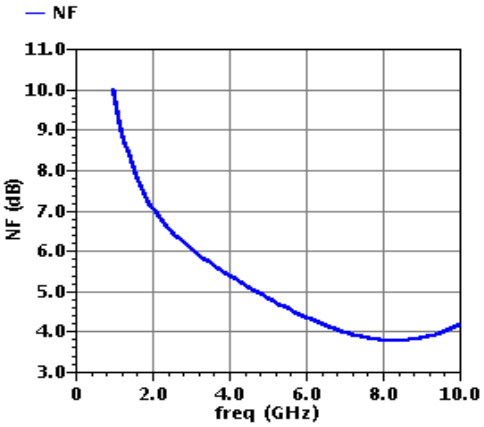

Fig. 15: NF of the second UWB LNA

Table 1: Circuit parameters of the first UWB LAN

	$(W/L)_1$	$(W/L)_2$	$(W/L)_3$	$(W/L)_4$
Transistor size	100/0.18	160/0.18	60/0.18	40/0.18
Resistor	R_1	RF, R_2	R_3	R_4
value	400 Ω	100 Ω	500 Ω	56 Ω
Inductor	L_1	L_2	L_3	-
value	0.4 nH	2.3 nH	2.8 nH	-

Table 2: Circute parameters of the second UWB LAN

	$(W/L)_{N,1}$	$(W/L)_p$	$(W/L)_2$	$(W/L)_3$	$(W/L)_4$
Transistor size	100/0.18	60/0.18	70/0.18	40/0.18	560/0.18
Resistor	R_F	R_1	R_2	R_3	-
value	180 Ω	90 Ω	100 Ω	56 Ω	-
inductor	L_{G1}	L_{G2}	L_1	L_2	-
value	0.7 nH	2.2 nH	1 nH	1.4 nH	-

Table 3: Performance summary and comparsion

Reference	(Huang *et al*., 2015)	(Kao and Chang, 2008)	(Chen *et al*., 2005)	This study
Technology	0.18 µm	0.18 µm	0.18 µm	0.18 µm
BW (Ghz)	3.1-10.5	3.1-10.6	3.1-10.6	3.1-10.6
Pdc (mW)	9.4	33.66	22.7	16
NF (dB)	5	5.8	4.12	3.7
S_{11} (dB)	<-8.6	<-9.6	<-9.7	<-10
S_{22} (dB)	<-8	<-9.5	<-8.4	<-10
S_{21} (dB)	9.5	11.7	11.4	15.2
FOM	3.5	0.93	2.38	5.3

CONCLUSION

It achieves a maximum power gain of 15.2 and 3.7 dB minimum NF. The power consumption is 16 mW from a 1.8 V supply.

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